SynTest Technologies
The *Testability* Company

@Speed

SynTest's Quarterly Newsletter
April 2006 Vol. 1

Welcome to the first April issue of the @Speed. This quarterly e-Newsletter gives you the latest news about SynTest corporation, products and solutions. For comments and suggestions, please contact info@syntest.com.

Contents:

Hot off the press ……	SynTest Engineers were busy publishing Technical Articles ……
DFT IP Strategy	*SynTest would proudly like to share a great news on Patents Approval ……*
Welcome Aboard our DFT IP licensing Program	No Designer Wants a Power-Hungry ATPG Test

Hot off the press ……

SynTest would like you to be a book worm

VLSI TEST PRINCIPLES AND ARCHITECTURES
Design for Testability
First Edition
By
Laung-Terng Wang, SynTest Technologies, Inc., Sunnyvale, CA, USA.
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http://elsevier.com/inca/707926

Audience
PRIMARY: Practitioners/Researchers in VLSI Design and Testing; Design or Test Engineers, as well as research institutes. SECONDARY: Undergraduate and graduate-level courses in Electronic Testing, Digital Systems Testing, Digital Logic Test & Simulation, and VLSI Design.

Contents
Chapter 1 – Introduction Chapter 2 – Design for Testability Chapter 3 – Logic and Fault Simulation Chapter 4 – Test Generation Chapter 5 – Logic Built-In Self-Test Chapter 6 – Test Compression Chapter 7 – Logic Diagnosis Chapter 8 – Memory Testing and Built-In Self-Test Chapter 9 – Memory Diagnostics and Built-In Self-Repair Chapter 10 – Boundary Scan and Core-Based Testing Chapter 11 – Analog and Mixed-Signal Testing Chapter 12 – Test Technology Trends in the Nanometer Age.

SynTest Engineers were busy publishing Technical Articles ……..

[1] L.-T. Wang, X. Wen, H. Furukawa, F.-S. Hsu, S.-H. Lin, S.-W. Tsai, K.S. Abdel-Hafez, and S. Wu, "VirtualScan: A New Compressed Scan Technology for Test Cost Reduction," *Proc. IEEE 2004 Int'l Test Conference (ITC-2004)*, pp. 916-925, Charlotte, NC, October 2004.

[2] X. Wen, T. Miyoshi, S. Kajihara, L.-T. Wang, K.K. Saluja, and K. Kinoshita, "On Per-Test Fault Diagnosis Using the *X*-Fault Model," *Proc. IEEE 2004 Int'l Conference on Computer-Aided Design (ICCAD-2004)*, pp. 633-640, San Jose, CA, November 2004.

[3] B. Cheon, E. Lee, L.-T. Wang, X. Wen, P. Hsu, J. Cho, J. Park, H. Chao, and S. Wu, "At-Speed Logic BIST for IP Cores," *Proc. IEEE 2005 Design, Automation and Test in Europe (DATE-2005)*, pp. 860-861, March 2005.

[4] X. Wen, Y. Yamashita, S. Kajihara, L.-T. Wang, K.K. Saluja, and K. Kinoshita, "On Low-Capture-Power Test Generation for Scan Testing," *Proc. IEEE 2005 VLSI Test Symposium (VTS-2005)*, pp. 264-270, May 2005.

Continued …..

[5] X. Wen, Y. Yamashita, S. Morishima, S. Kajiihara, L.-T. Wang, K.K. Saluja, and K. Kinoshita, "A Method for Low-Capture-Power At-Speed Test Generation," *Proc. 6th IEEE Workshop on RTL and High Level Testing*, pp. 40-49, Harbin, China, July 2005.

[6] L.-T. Wang, X. Wen, P.-C. Hsu, S. Wu, and J. Guo, "At-Speed Logic BIST Architecture for Multi-Clock Designs," *Proc. IEEE 2005 Int'l Conf. on Computer Design (ICCD-2005)*, pp. 475-478, October 2005.

[7] L.-T. Wang, K.S. Abdel-Hafez, X. Wen, B. Sheu, S. Wu, S.-H. Lin, and M.-T. Chang, "UltraScan: Using Time-Division Demultiplexing/Multiplexing (TDDM/TDM) with VirtualScan for Test Cost Reduction," *Proc. IEEE 2005 Int'l Test Conf. (ITC-2005)*, Paper 36.4, (8 pages), November 2005.

[8] X. Wen, Y. Yamashita, S. Morishima, S. Kajihara, L.-T. Wang, K.K. Saluja, and K. Kinoshita, "Low-Capture-Power Test Generation for Scan-Based At-Speed Testing," *Proc. IEEE 2005 Int'l Test Conf. (ITC-2005)*, Paper 39.2, (10 pages), November 2005.

[9] S. Wu, L.-T. Wang, J. Cho, Z. Jiang, and B. Sheu, "Test Compression and Logic BIST at Your Finger Tips," *Proc. IEEE 2005 Int'l Test Conf. (ITC-2005)*, Panel 5.1, (2 pages), November 2005.

DFT IP Strategy

At SynTest, we have seen great successes from our global customers in the applications of these technologies to their designs in the US, Japan, Korea, Taiwan, and Israel. Our customers have advised us that a single site licensing of these technologies at an affordable fee could benefit more of the electronics industry, and of course, end-users.

Offering a "bundle" of their overall products (for a complete solution flow from architecture to implementation of designs, including DFT tools) at an attractive price has been a common technique used by all major vendors to entice end-users to embrace their own tools and flow. It is difficult to identify pricing of each of the point tool (e.g. DFT) in such attractively priced bundle. This presents a very difficult challenge to small vendors who only provide point tools in specific areas. SynTest is now countering that by expanding our DFT tools bundle with addition of a site license for all our DFT IP – current and future.

SynTest started receiving approval for some fundamental patents in the last quarter of 2005 from the US and European patent offices. With these patent approvals, SynTest embarked on a transition to become a DFT IP licensing company. This transition was announced at the IEEE International Test Conference (ITC) held in Austin, Texas, in Nov. 2005, and will continue for one year (through 2006). SynTest DFT IP is available for three years term for an annual license fee that follows a 3-tier pricing model proportional to the annual revenue of the licensee company. During promotional period, full SynTest DFT tool suite is being included free of charge in the DFT IP license.

SynTest would proudly like to share a great news on Patents Approval ……

SynTest Receives A Fundamental Patent for At-Speed Capture Invention for Logic BIST

"Multiple-capture DFT system for Detecting or Locating Crossing Clock-domain faults during Self-test or Scan-test"

SAN JOSE, Calif., Feb 28, 2006 -- SynTest Technologies, Inc., a leading supplier of Design-for-Test (DFT) tools, was granted 30 claims on Feb. 28, 2006 under United States patent number 7,007,213 for its invention of At-Speed capture for detection of faults using Logic BIST DFT scheme for multiple clock domain designs.

Please read on by clicking on the following link **…...**
http://www.syntest.com/PressReleaseArchive/PR_At-Speed-LBIST_Patent_final.pdf

You can also find PR announcements of the other two patents approval received in 2005 by SynTest ….

SynTest Receives "Computer-aided design system to automate scan synthesis at register-transfer level" Patent for RTL Scan Synthesis Invention

SynTest Receives "Multiple-capture DFT system for scan-based integrated circuits" Patent for At-Speed Scan/BIST Invention

As of March 31, 2006, SynTest has 3 patents issued, 2 patents allowed, and 20+ patent applications pending.

Welcome Aboard our DFT IP Licensing Program

SynTest would like to welcome 10 new partners into the promotional DFT IP licensing program in Q4 2005 and Q1 2006. New and renewal customers of licensing individual DFT software are not counted:

USA – 5
Korea – 3
Taiwan – 2

Thank You Very Much!!!

No Designer Wants a Power-Hungry ATPG Test

By Dr. Jake Jiang, SynTest USA

Power dissipated during chip testing mainly consists of two components, shift power and capture power. Shift power is the power dissipated during the shift phase, when vectors are scanned in or responses are scanned out through scan cells, while capture power is the power dissipated during the capture phase, when memory elements in the circuit are either captured once, in the case of testing stuck-at faults, or twice, in the case of testing delay faults. If uncontrolled, test power can go beyond the package limit and damage the chip. Even if the chip is not damaged, elevated test power can also cause yield loss due to IR drop. Thus, it is desirable to estimate test power dissipated during shift and capture phases and reduce it to an acceptable level.

Test power reduction can be done in two distinct phases during scan ATPG:

1. **Shift power reduction** - Shift power can be reduced with power-conscious test scheduling and by generating low-shift-power vectors. Filling blocks of X's in the generated vectors with the same value to lower the resultant shift power can generate low-shift-power vectors. Since more X's may be needed for X-filling to achieve enough power reduction, the level of test compaction may have to be reduced to satisfy given power requirements. Tradeoffs between test data volume and test power are to be made. Also "01" and "10" transitions at different positions of a vector have different contributions to shift power. This can be used to direct ATPG to place more X's at highly power-affected positions. More advanced test generation techniques, such as using shift power as an ATPG branch-and-bound search condition, can also be used.

2. **Capture power reduction** - High capture power can cause yield loss due to IR drop. Capture power can be reduced by reducing transitions at memory elements during capture. For stuck-at ATPG, each memory element in the circuit is captured once. To reduce power, X's in the generated vectors can be filled in such a way that values at memory elements are made to stay the same before and after capture. For transition ATPG, each memory element is captured twice for each applied vector. So for each memory element, both captures have to be taken into consideration to produce an overall low capture power.

TurboScan and VirtualScan Low-Power ATPG (currently under beta test)

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