VirtualScan™

TOOL SUITE FOR SCAN COMPRESSION SYNTHESIS AND ATPG

Today, integrated chips with multi-million gates, containing logic, memory and analog functions, are becoming commonplace. At the same time, meeting tight time-to-market schedules, controlling costs and maintaining high quality standards are critical to the success of any such Integrated Circuit (IC) development.

Design-for-Test (DFT) tools and methodologies enable automation of many aspects of the IC structural testing process, ensuring that the chip comes through tape-out and manufacturing on time and according to specifications with acceptable level of quality. Among the various DFT methodologies available today for structural testing, scan insertion with Automatic Test Pattern Generation (ATPG) is the most preferred DFT methodology.

However, semiconductor testing cost has been increasing steadily over the years such that today it is a major part of the overall manufacturing cost of chips. The rapidly increasing size and complexity of new chips calls for a radical approach to enable companies developing million-gate System-on-Chips (SOCs) to speed their products through the test process more rapidly without having to upgrade to more expensive, next generation Automatic Test Equipment (ATE) or expand existing ATE scan pattern memory.

The diagram in this page shows the relationship between a Chip-Under-Test (CUT), the test data generated, and the ATE. On one hand, the ATE limitations include limited number of scan pins, limited amount of scan pattern memory, high per-pin cost as well as high per-MHz cost. On the other hand, new SOC designs are larger in size, have complex functionality, limited number of I/O pins and due to shrinking geometries need to test more various types of defects, calling for bigger pattern sizes, longer scan chains and ever-increasing test data volumes to attain high fault coverage. However, bigger pattern sizes need more scan pattern memory and longer scan chains need longer test time, both resulting in higher test costs.

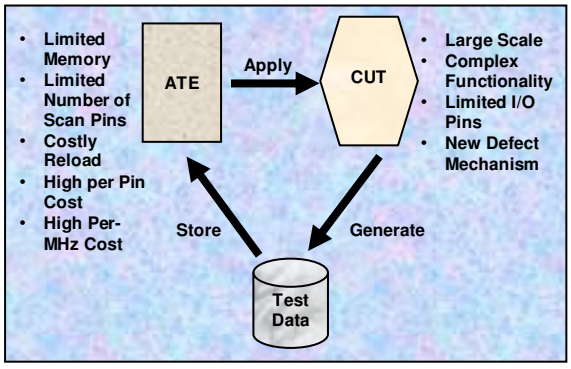
VirtualScan™ is SynTest's solution to combat this increase in test data volume and test cycle volume. With VirtualScan™ an extremely large number of short scan chains within the SOC can be virtually accessed from outside the chip with a limited number of pins assigned as scan pins. Inside the chip, SynTest's patented circuitry is used to broadcast each external scan-input chain to a user-selectable number of internal scan chains and at the other end, compact them into the original number of external scan chains. An evaluation on a 2-million gate design using VirtualScan™ showed a 22x reduction in test time. Further, the static and dynamic compaction capabilities of SynTest's powerful ATPG tool help reduce pattern sizes, leading to overall reduction in test costs.

BENEFITS OF VIRTUALSCAN™

- Reduces cost of semiconductor testing – 5x to 50x
- Extends life of existing ATE for large SOC designs
- Smaller test data volume and shorter test time
- Short test development time with no iterations
- High fault coverage
- Predictable and very low hardware overhead
- Smooth migration into existing scan ATPG flow
- Diagnosis support

FEATURES OF VIRTUALSCAN™

- Uses a patented virtual scan technology for broadcasting external scan chains to a user-selectable number of shorter internal scan chains and compacting them back into original number of external scan chains
- Automatically inserts broadcaster and compactor circuitry
- Includes tools for scan insertion and synthesis
- Outputs a complete VirtualScan netlist
- Has a built-in enhanced VirtualScan ATPG
- Supports static and dynamic compaction of ATPG patterns
- Applies advanced multiple clock domain handling using a proprietary multiple-capture-per-cycle scheme
- Supports scan chains inserted using third party tools
- Is fully compatible with SynTest's other DFT products as well as TurboDiagnosis for scan failure analysis, debug, and diagnosis



TEST COST REDUCTION

In a scan test environment, the test cost depends on the test data volume and the test cycle volume.

The test data volume determines the pattern memory required on an ATE. To process increasingly large amounts of test data volumes, the options are either to increase pattern memory size, which is expensive, or run reloads on the ATE, which means more time spent on ATE usage, again resulting in increased costs.

The figure alongside illustrates the relationships that affect these test costs, where

N = Number of scan test patterns

L = Scan chain length

W = Width of stored patterns

W is fixed; hence, to reduce the test costs we need to reduce both **N** and **L**.

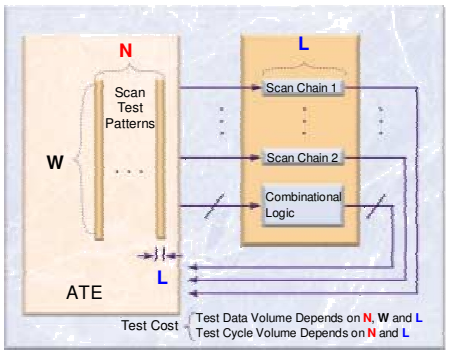
To generate very compact ATPG patterns, SynTest uses proprietary static and dynamic compaction techniques in its ATPG tool.

In static compaction, reverse fault simulation and a minimal cover set algorithm are used to choose the best test pattern, which can detect the same hard detected faults, thereby reducing the total number of test patterns generated.

In dynamic compaction, a proprietary algorithm is used to target secondary faults, while patterns are being generated, until most unknowns in a test pattern are filled with known values. This again increases the utilization of 'intelligent' test patterns and consequently reduces the total number of test patterns generated.

Further, SynTest's multiple-capture-per-cycle scheme for ATPG slashes the total test time of designs with multiple-frequency clock domains, as only one scan-in/scan-out phase is deployed for each pattern. Though the multiple-capture-cycle takes a little longer than the capture cycle for schemes based on one-hot clock, it is much shorter than the cumulative time taken by the scan-in and scan-out operations for individual clocks, thereby offering a test compaction factor almost equal to the total number of clock domains.

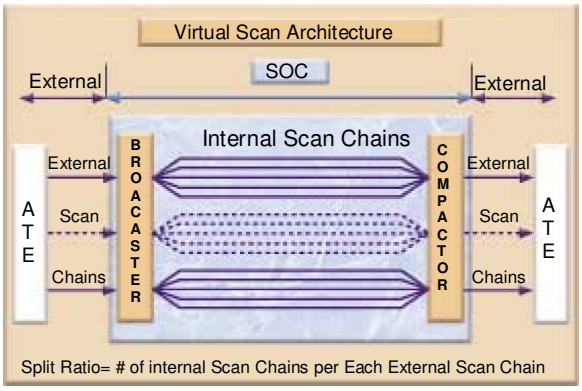
The limitations on the number of scan pins available on an ATE forces longer scan chains to be used for larger and more complex SOC designs.



The longer the scan chains, the more time it takes to apply test patterns on the ATE. Hence, a solution is to use a large number of shorter scan-chains to circumvent the limitation of the number of scan test pins available on the ATE.

With SynTest's VirtualScan™ technology, the long scan chains are 'split' into shorter chains. Users select a 'Split Ratio' as the ratio between the external scan chain count and the internal scan chain count. The resultant large number of short scan chains within the SOC can then be virtually accessed from ATE scan test pins. Inside the chip, SynTest's patented circuitry broadcasts each external scan-input chain values to the internal scan chains, and at the other end, compacts captured results back to the original number of external scan chains.

VirtualScan™ contains an automatic synthesizer to incorporate the ***Broadcaster*** and ***Compactor*** into the scan circuitry and uses an enhanced virtual scan ATPG technology to generate the 'compressed' test patterns.



VIRTUALSCAN FLOW

The VirtualScan™ flow starts with a synthesized gate-level netlist. SynTest recommends running TurboCheck-Gate™ to check and repair testability violations, if any.

Scan Synthesis

VirtualScan™ contains tools for scan chain synthesis, where it selects scan flip-flops based on clock domains, and reorders and stitches the flip-flops for minimum scan chain routing overhead. A gate-level scan chain inserted netlist then is generated.

VirtualScan™ also accepts a netlist with scan implementation done by a 3rd party tool. If this is preferred, it is still recommended to check for DFT violations. Scan extraction is performed on the gate-level scan-inserted netlist.

Virtual Scan Synthesis and ATPG

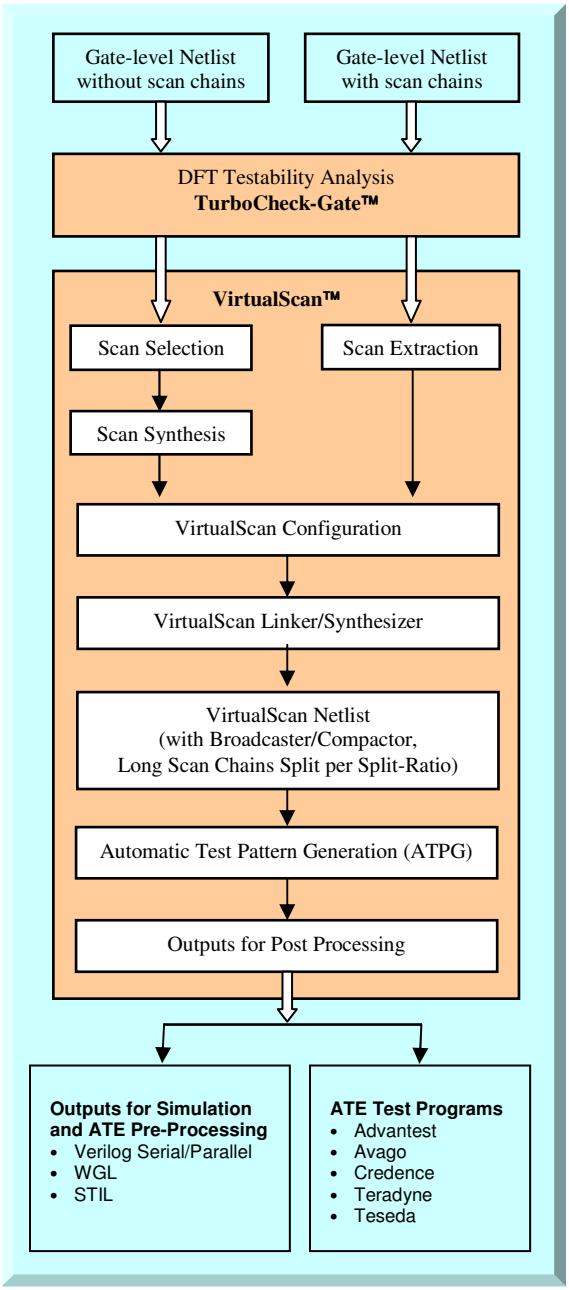
For an already-scanned netlist, the flow processes user-specified virtual scan configuration specification. Then a linker incorporates the ***Broadcaster*** and ***Compactor*** into the scan circuitry, and the scan chains are split into a number of internal scan chains based on the user-definable "Split Ratio." This new netlist, the VirtualScan netlist, is created and has an extremely low area impact because the Broadcaster and Compactor are pure combinational logic.

Next, the VirtualScan™ ATPG tool uses an enhanced virtual scan ATPG technology to generate very high fault coverage, compressed scan test patterns for manufacturing test. Users can run ATPG by setting the circuit in either virtual scan mode or serial scan mode.

For Engineering-Change-Order (ECO), users only need to rerun ATPG to generate new patterns. The compression netlist remains unchanged.

Outputs

Available ATPG output formats are Verilog Serial/Parallel, WGL and STIL. Supported output formats for ATE are for Advantest, Avago, Credence and Teradyne.



RELOADS

"Reloads" on an ATE depend on the ATE pattern memory size and the Test Data Volume. Reducing Test Data Volume reduces the pattern memory size required and the number of "Reloads."

VirtualScan™ is fully compatible with SynTest's other DFT products.

OTHER PRODUCTS FROM SYNTEST

TuroboScan™ is SynTest's flagship solution to Automatic Test Pattern Generation that uses patented algorithm for smart capture and generates compacted patterns for stuck-at, transition, path delay, and bridging faults. Also available is a feature for low power patterns with minimal toggles during scan shift and capture.

UltraScan™ is SynTest's solution to reduce test time by 50x to 500x. It is used along with VirtualScan™ to reduce the overall test cost. UltraScan™ extends life of existing ATE for testing large SOC designs. With UltraScan™ a small number of high-speed I/O pads are adequate to run a scan ATPG test for a design with a large number of internal scan chains of shorter length. It achieves test pin reduction through proprietary TDDM/ TDM circuitry. Overall shorter test load times are realized by taking advantage of the unutilized bandwidth available on high-speed channels on the ATE during low-speed scan-shift operation.

TurboCheck™ is a suite of RTL and gate-level DFT rule analysis tools. At RTL it identifies testability problems at the earliest stage of the design cycle, even before synthesis, preventing costly and time-consuming iterations in the design process. At gate-level, it analyzes designs with or without scan, for DFT testability. It uses a set of rules to identify and report problems that cause low fault coverage. Both offer optional DFT rule repair capability.

TurboBIST-Logic™ is a tool suite for logic Built-In Self-Test (BIST) that helps reduce ATE tester costs during production, and enables testability logic re-use at board, system level and in the fields. It is ideal for SOC designs with multi-million gates/primitives, multiple clock domains, and multiple and high frequencies. It detects timing faults by using "true at-speed' testing – a patented capture scheme. It helps reduce test preparation time and test costs when using multiple instantiation of "legacy" logic circuit blocks or re-using IP cores in different designs. It is ideal for in-field remote testing or non-invasive testing, prototype debug/diagnosis and for the wafer sorting process.

TurboBIST-Memory™ is a memory BIST tool for embedded memories including SRAM and ROM. It enables simultaneous multiple BIST memory tests via a shared controller. It outputs synthesizable RTL BIST controllers and logic synthesis scripts. It also generates a Verilog test bench automatically. It also supports programmable algorithm and self-repair for SRAM.

TurboBSD™ is a Boundary-Scan test tool suite that performs IEEE 1149.1 and 1149.6 compliant Boundary-Scan logic synthesis, generates Boundary-Scan Description Language (BSDL) files, and Boundary-Scan test patterns, including verification and parametric test benches. It outputs netlists in RTL & Gate-level in Verilog.

TurboDFT™ is a tool for design modification and integration. It eliminates the tedious, error-prone manual design netlist modification process by automatically cut-connect, stitch and integrate any combination of hierarchy and DFT cores, such as scan cores, memory BIST, logic BIST, and IP, and Boundary-Scan (JTAG) core.

ORDERING INFORMATION

TurboScan™, VirtualScan™, UltraScan™: For Scan Synthesis and ATPG for stuck-at faults. Plus select test program format for one ATE.

Options:

TurboScan-TR™: For transition faults ATPG
TurboScan-LP™: For low power ATPG
TurboScan-PD™: For path delay ATPG
TurboScan-BF™: For bridging fault ATPG

Other Products from SynTest

- **TurboBSD™, TurboBIST-Memory™, TurboDFT™, TurboCheck™, TurboBIST-Logic/Memory™, TurboFault™, TurboDiagnosis™, TurboDeskTopDebugger™**
- **DFT-PRO Plus™:** A comprehensive package of DFT tools which includes VirtualScan™, TurboBSD™, TurboBIST-Memory™, TurboDFT™, and TurboCheck™:

PLATFORMS

VirtualScan™ runs on Linux platforms.

OTHER PRODUCTS FROM SYNTEST

TurboFault™ is a concurrent fault simulator useful where scan/ATPG technology cannot be used or to enhance fault coverage on top of scan/ATPG technology. It is the fastest high capacity concurrent fault simulator based on SynTest's proprietary algorithms in fault simulation technology. With its low memory consumption, user-definable fault detection criteria, fault-tracing, back-tracing and crash recovery capabilities, it combines high performance with versatility and accuracy. It accepts fault lists from most ATPG tools. As input stimuli, it can handle VCD, WGL and Novas FSDB.

TurboDiagnosis™ & TurboDeskTopDebugger (TDTD)™ are diagnosis tool and desk-top device debugger for when physical ICs with scan and/or BIST failed or are found to have mismatches with expected outputs during testing.

PATENTS SynTest products are protected by one or more of the patents listed in http://syntest.com/patent.htm.

Patents pending in the U.S. and other countries.

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