

Tool Suite to Reduce Cost of Testing for Nanometer Technology ASICs



SYNTEST

The Testability Company

Today, integrated circuits (ICs) with multi-million gates, containing logic, memory and analog functions are becoming commonplace. At the same time, meeting tight time-to-market schedules, controlling costs and maintaining high quality standards are critical to the success of any such new IC development. Further, nanometer technology is a reality.

However, the cost of semiconductor testing has been increasing steadily over time making it a major part of the overall chip manufacturing cost. The increase in size and complexity of new chips calls for a radical approach to enable companies developing million-gate Application-Specific ICs (ASICs) to speed up their product development through the test process more rapidly without having to upgrade to more expensive, latest generation Automatic Test Equipment (ATE) or to expand pin-electronics on existing ATE.

For ASICs designed with feature size greater than 130 nm, testing for stuck-at faults and I_{DDQ} is adequate to ensure acceptable quality levels. However, in ASIC's designed for 130 nm or below, many manufacturing defects are no longer static. They become delay defects and it becomes necessary to use delay tests to detect the transition faults and path delay faults. Often bridging fault tests are also required. Since these delay tests are more complicated than tests for stuck-at faults, many more test patterns are required resulting in more time on ATE and more memory to store test patterns. The end result is increased test cost. It is in this environment that UltraScan together with VirtualScan help in reducing the cost of ASIC testing.

UltraScan with its Time-Division De-Multiplexing (TDDM) and Multiplexing (TDM) circuits takes advantage of the unutilized bandwidth available on high-speed channels on the ATE during low speed scan-shift operation, and thereby enables overall shorter load times of scan chains. Furthermore, today's ASIC designs operate at significantly higher speeds and require that their high-speed I/O pads are tested at proper speed.

resulting in higher test cost. Hence, any method for testing these high-speed I/O pads "at-speed" by utilizing bandwidth available on high-speed channels on the existing ATE helps towards reducing test costs. Here again UltraScan helps in this at-speed test of high-speed I/O pads; and, at the same time, it assists in preserving test structures used for test data volume compression. Through the pin reduction realized with TDDM/TDM, a small number of high-speed I/O pads are sufficient to run a scan-ATPG test for a design with a large number of internal scan chains of shorter length.

Thus, UltraScan is primarily used with SynTest's VirtualScan product to further reduce test application time. SynTest's VirtualScan itself offers a significant reduction in the cost of semiconductor testing by reducing test data volume and test cycle volume by 5x – 50x, thereby reducing the necessity of adding expensive memory on ATE. An evaluation on a 4.2-million gate circuit showed a reduction in test time of 18.7x through VirtualScan and an additional reduction of 10x through UltraScan, giving a total reduction in test time of 187x.

UltraScan™ with VirtualScan™

- Reduces test data volume of semiconductor testing – 5x to 50x
- Reduces test time – 50x to 500x
- Extends life of existing ATE for SOC
- Reduces test time for all scan designs with ATPG compression structures
- Further shortens overall test load times by taking advantage of the unutilized bandwidth on high-speed channels on the ATE during low-speed scan-shift operation
- A small number of high-speed I/O pads adequate to run a scan ATPG test for a design with a large number of internal scan chains of shorter length
- Pin reduction through TDDM/ TDM
- High fault coverage
- Better delay fault coverage for high-speed I/O pads on the device
- Short development time, no iterations
- Predictable & low hardware overhead
- Smooth migration into scan ATPG flow
- Diagnosis support

Features of VirtualScan™

- Uses patented technology for broadcasting external scan chains (ATE channels) to many shorter internal scan chains and compacting them back to original number of external scan chains.
- Outputs complete VirtualScan netlist
- Uses an enhanced VirtualScan ATPG, that also performs static and dynamic pattern compaction
- Supports multiple clock domain handling with patented multiple-capture-per-cycle scheme
- Handles scan chains inserted by 3rd party tools
- Is fully compatible with SynTest's existing DFT tools as well as TurboDiagnosis product line for failure analysis, debug, and diagnosis of scan chains.

The UltraScan Architecture

The UltraScan architecture consists of three major parts:

- A Time-Division De-Multiplexing (TDDM) circuit placed between high-speed I/O pads for driving scan chains and the internal VirtualScan broadcaster input ports
- A Time-Division Multiplexing (TDM) circuit placed between the internal VirtualScan compactor output ports and high-speed I/O pads to bring out scan chains
- VirtualScan broadcaster and compactor circuits

The TDDM, TDM, broadcaster and compactor circuits are generated as Register Transfer Level (RTL) blocks. These RTL blocks are then synthesized along with the design's RTL codes and other DFT RTL blocks into a gate-level netlist. As these blocks are at RTL, it eases the design floor-planning decisions carried out at the RTL stage.

The TDDM circuit uses a high-speed clock to demultiplex the high-speed scan data into scan chains operating at a slower data rate for scan shift.

Following the TDDM circuit, the VirtualScan broadcaster is used to broadcast the scan data into multiple VirtualScan scan chains depending on the split ratio. This allows designers to compress the test data volume and test cycles used to test the device. This compression comes on top of the test cycle reduction, measured using the scan shift clock, as the result of the time-division demultiplexing of the high-speed scan data.

The compactor to compact the captured scan data follows the VirtualScan scan chains. The outputs of the compactor are then used to drive the TDM circuit, which is again operated at the high-speed clock, to multiplex the captured scan data back into high-speed captured scan data for comparison on the ATE. This circuit architecture allows designers to achieve further reduction in test cycles, measured

using the scan shift clock, on top of the VirtualScan test cycle and test data volume reduction, further reducing overall test cost.

VirtualScan uses an enhanced, proprietary scan ATPG technology to generate compressed test patterns. It contains a fast combinational ATPG that generates very high fault coverage test patterns.

PATENTS

SynTest products are protected by one or more of the patents listed in <http://syntest.com/patent.htm>.

Patents pending in the U.S. and other countries.

