TurboScan

TOOL SUITE FOR SCAN SYNTHESIS AND ATPG

Today, integrated circuits (ICs) with multi-million gates, containing logic, memory and analog functions are becoming commonplace. At the same time, meeting tight time-to-market schedules, controlling costs and maintaining high quality standards are critical to the success of any such new IC development.

Design-for-Test (DFT) tools and methodologies enable automation of many aspects of the IC structural testing process, ensuring that the chip comes through tape-out and manufacturing on time, and meeting target quality. DFT tools enable creation of efficient test patterns that detect most major manufacturing defects. Effective DFT methodologies available today for structural testing include scan/scan-compression synthesis and ATPG (Automatic Test Pattern Generation), logic BIST (Built-in Self-Test) and fault simulation.

TurboScan is an advanced full-scan test suite, including a scan synthesizer and an ATPG. The scan synthesizer supports full scan methodologies. The ATPG engine uses advanced search and compaction algorithms to produce very high fault coverage test patterns with very concise pattern sizes.

SYNTEST
The Testability Company

Benefits of TurboScan

Improves design quality through very high fault coverage test patterns

Generates stuck-at, transition, bridging fault, I_{ddq}, path-delay, and low-power test patterns

Reduces test costs - shorter test times and reduced test data volumes

Integrates easily into existing design flow

Allows for ATPG for designs done by 3rd party scan synthesis tools.

Minimizes silicon usage/overhead

Runs with short CPU Times

TurboScan ATPG algorithms also work on asynchronous sequential circuits containing gated clocks, RAMs, ROMs, tri-state gates, asynchronous set/reset functions, and unidirectional transistors. It detects static and timing related defects.

TurboScan uses an advanced 64-value search algorithm. This reduces the ATPG search space, especially for circuits containing non-scan flip-flops or other uncontrollable signal sources, and thereby improves the speed of the ATPG process and the circuit's fault coverage.

SynTest's patented multiple-capture-per-cycle scheme for ATPG significantly reduces the total test time of designs with multiple-frequency clock domains, as only one scan-in/scan-out phase is deployed for each pattern.

Proprietary static and dynamic compaction algorithms are used to generate very compact ATPG patterns. These help reduce ATE test costs, by reducing test time and avoiding reloading of patterns.

TurboScan generates patterns for commonly used fault models e.g. Stuck-at, Transition Delay, Bridging Fault, Path Delay, Low Power, etc. The transition delay fault model needs an extra capture clock edge to detect a signal slow-to-rise or slow-to-fall. So there are two captures within the capture window. It is often called double-capture. The first capture clock launches a transition, then at the second capture clock edge, the scan chain captures the delay effect. The time between the first and the second clock edges can test the at-speed effect of the device. An extended feature is test patterns for the path-delay faults of user given set of path(s). A path-delay fault is defined as a path (from a flip-flop output to a flip-flop input) being slow to rise or fall. Normally, users derive those paths, which are timing critical paths, from a static timing analysis tool.

For low power devices, ATPG also generates patterns for low power devices with minimal toggles during shift operation as well as minimal power in capture cycles.

FEATURES

Combinational ATPG
  Contains cycle-based good and fault simulation engines for fault detection.
  Stuck- at, transition, bridging fault, Iddq, path-delay patterns Multi- Capture for reduced test pattern and power dissipation Patented At-Speed capture scheme

Multi- Cycle-Path Support
  Multi- Detection (N-Detect) for higher test quality Low power support by minimal toggle
  Static & Dynamic test compaction for test pattern reduction Smart-Capture for ATPG time reduction.

Post-ATE diagnosis capabilities
  Uses 64-value search algorithm to improve speed and fault coverage Scan Synthesis and Debug
  - Automatic identification and repair of testability rule violations
  - Scan cell insertion
  - Scan chain synthesis based on clock domains and/or power domains
  - Scan chain extraction support in case of already-scanned netlist
  - Scan chain debug utilities

Flexible transparent/non-transparent latch options
  - No overhead, no potential timing violations, no potential feedback loops, clock fault detection

Non-scan positive/negative flip-flops
  - Can propagate values from D/S/R to Q
  - Fewer undetectable faults (including clock faults) Multiple internal/external clocks
  - Groups and orders clocks, and generates each test pattern to capture results of all ordered clock groups within one extended capture window.

Smart tri-state bus handling
  - Contention free behavior before and after capture
  - No need to run fault simulation after ATPG to drop patterns
  Sophisticated Multiple and Multi-port RAM support
  - Black box, bypass and wrapper modes
  Advanced compaction algorithm
  - Static and dynamic compaction
  - Compacted pattern sizes - reduce test costs
  ATPG outputs for post-processing are available
  - in standard formats: Verilog Serial/Parallel, WGL, or STIL
 - for specific ATE testers, such as Advantest, Avagot, Credence, Teradyne, or Teseda

TurboCheck-Gate (Companion product):

It analyzes a gate-level design with or without scan, for DFT testability rule violations. It calculates the controllability and observability for designs assuming non-scan, partial-scan or full-scan implementation. It uses a set of rules to identify and report problems that may cause low fault coverage.

DESIGN FLOW

A gate-level netlist is first run through TurboCheck-Gate to check for DFT violations. It is then fed to TurboScan where scan flip-flop selection and scan chain synthesis are performed. The scan-inserted netlist is then fed to the ATPG for test pattern generation. The test patterns can be output in a number of different formats for post processing and use on Automatic Test Equipment (ATE).

TurboScan can also work with gate-level netlists that have scan chains already inserted into them by other commercially available scan synthesis tools. In this case also the gate-level netlist is first checked for DFT violations, using TurboCheck-Gate. Then scan extraction is performed to obtain relevant scan information. The scan-inserted netlist is then fed to the ATPG for test pattern generation, as mentioned above.
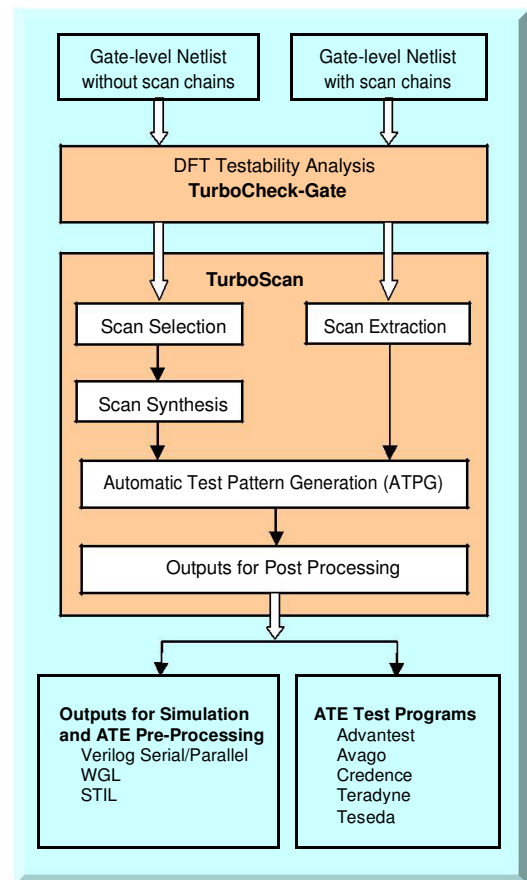
SCAN TEST FOR MULTIPLE-CAPTURE-PER-CYCLE SCHEME

SynTest's multiple-capture-per-cycle scheme for Automatic Test Pattern Generation slashes the total test time of designs with multiple-frequency clock domains, as only one scan-in/scan -out phase is deployed for each pattern.

Figure 1 shows a simple circuit with only one scan chain and the basics of scan test for a single-frequency design. Here, the total test time for scan testing depends on the amount of time needed for each scan pattern test and on the total number of scan test patterns.

This can be extended to a multiple-frequency design by identifying scan flip-flops in each clock frequency domain and forming a scan chain or multiple scan chains for each frequency (Fig. 2). In the normal operational mode of a chip, many of these clock domains mutually interact, and this can occur at different asynchronous moments (called interclock-domain activity). Such "external" clock-domain interaction can result in instabilities, and thus invalidates the capture-cycle results. As is well documented, ATPG schemes based on combinational logic handling will not be able to handle such interactions. Consequently, a hold mode or isolation circuit typically is employed in such schemes to ensure the accuracy of results during the capture cycle of each scan chain.

In this case, scan pattern values are scanned in for all chains, but only one clock domain, called the "One-hot clock" with one scan chain, is used in the testing during the capture cycle. The process starts with one frequency domain, and all other clock domains are placed in a hold, or inactive, mode. The results are scanned out and the process is repeated for the rest of the clock domains. As can be seen, the test time needed for each pattern equals the number of clock domains multiplied by the time for each pattern to scan in, go through capture, and scan out. This result then is multiplied by the number of patterns for the full scan test.

SynTest's multiple-capture-per-cycle scheme is shown in Figure 3. Scan pattern values are scanned in for all scan chains, a multiple-capture-per-cycle follows, and the final results are scanned out. The resulting total test time for a scan pattern is given by the time for each pattern to scan-in, its additional time for the multiple-capture interval and the time needed to scan out. Note that the multiple-capture-per-cycle takes a little longer than the capture cycle for schemes based on one-hot clock, but is much shorter than time taken by the scan-in and scan-out operations. Thus, the test compaction factor equals the total number of clock domains.
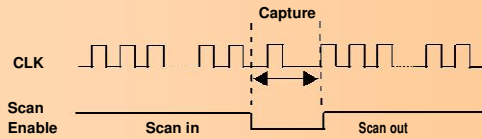

Fig. 1 – Time required on a tester to process a single scan chain

Test time $[t_{sc}] = [t_{sin}] + [t_{cap}] + [t_{sout}]$ Where:
t_{sc} = time required to process a single scan
t_{sin} = time required to input (load) a scan chain t_{cap} = time required for a capture-cycle
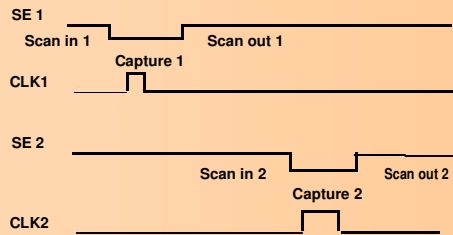t_{sout} = time required to output (unload) a scan chain

Fig. 2 – Time required on a tester to process multiple scan chains, assuming all scan chains are of the same length

Total test time $[t_{tot}] = [n_{sc}]^* [t_{sc}] = [n_{sc}]^*[t_{sin} + t_{cap} + t_{sout}]$
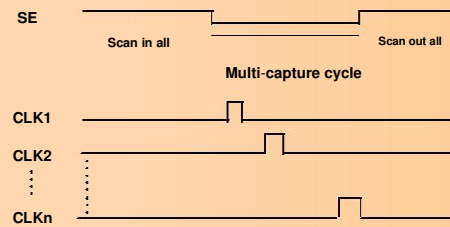Where: n_{sc} = number of scan chains being processed

Fig. 3 – Time required on a tester to process multiple scan chains using SynTest's proprietary "multiple-capture-per-cycle" methodology

Total test time $[t_{syn-tot}] = [t_{sin}] + [n_{sc}]^*[t_{mcap}] + [t_{sout}]$
Where: t_{mcap} = time required for a multi-capture-cycle

Since $[t_{sin}]$ or $[t_{sout}]$ are $>> [t_{cap}]$; and $[t_{mcap}] \sim = [t_{cap}]$, the test time required to process multiple scan chains using SynTest's proprietary "multiple-capture-per-cycle" methodology is only $1/[n_{sc}]$ the time required for conventional processing.
Thus, the saving in test time using multi-capture-per-cycle is $[n_{sc}]$.

OTHER PRODUCTS FROM SYNTEST

VirtualScan™ is SynTest's solution to combat a surge in test data volume and test cycle volume. Up to 50x compaction is achievable with VirtualScan™. An extremely large number of short scan chains within the SOC can be virtually accessed from outside the chip with a limited number of pins assigned as scan pins. SynTest's circuitry is used to broadcast the original external scan-input chains to a user-selectable number of internal scan chains and then compact results into the original external scan- output chains.

UltraScan™ is SynTest's solution to reduce test time by 50x to 500x. It is used along with VirtualScan™ to reduce the overall test cost. UltraScan™ extends life of existing ATE for testing large SOC designs. With UltraScan™ a small number of high-speed I/O pads are adequate to run a scan ATPG test for a design with a large number of internal scan chains of shorter length. It achieves test pin reduction through proprietary TDDM/ TDM circuitry. Overall shorter test load times are realized by taking advantage of the unutilized bandwidth available on high-speed channels on the ATE during low-speed scan-shift operation.

TurboBIST-Logic is a tool suite for logic Built-In Self-Test (BIST) that helps reduce ATE tester costs during production, and enables testability logic re-use at board, system level and in the fields. It is ideal for SOC designs with multi-million gates/primitives, multiple clock domains, and multiple and high frequencies. It detects timing faults by using "true at-speed' testing – a patented capture scheme. It helps reduce test preparation time and test costs when using multiple instantiation of "legacy" logic circuit blocks or re-using IP cores in different designs. It is ideal for in-field remote testing or non-invasive testing, prototype debug/diagnosis and for the wafer sorting process.

TurboBIST-Memory is a memory BIST tool for embedded memories including SRAM and ROM. It enables simultaneous multiple BIST memory tests via a shared controller. It outputs synthesizable RTL BIST controllers and logic synthesis scripts. It also generates a Verilog test bench automatically. It also supports programmable algorithm and self-repair for SRAM.

TurboBSD is a Boundary-Scan test tool suite that performs IEEE 1149.1 and 1149.6 compliant Boundary-Scan logic synthesis, generates Boundary-Scan Description Language (BSDL) files, and Boundary-Scan test patterns, including verification and parametric test benches. It outputs netlists in RTL & Gate-level in Verilog.

TurboCheck is a suite of RTL and gate-level DFT rule analysis tools. At RTL it identifies testability problems at the earliest stage of the design cycle, even before synthesis, preventing costly and time-consuming iterations in the design process. At gate- level, it analyzes designs with or without scan, for DFT testability. It uses a set of rules to identify and report problems that cause low fault coverage. Both offer optional DFT rule repair capability.

TurboDFT is a tool for design editing and integration. It eliminates the tedious, error-prone manual design netlist editing process by automatically cut-connect, stitch and integrate any combination of hierarchy and DFT cores, such as scan cores, memory BIST, logic BIST, and IP, and Boundary-Scan (JTAG) core.

PLATFORMS TurboScan runs on Linux platforms.

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ORDERING INFORMATION

TurboScan , VirtualScan , UltraScan : For Scan Synthesis and ATPG for stuck-at faults. Plus select test program format for one ATE. Options:

TurboScan-TR : For transition faults ATPG

TurboScan-LP : For low power ATPG

TurboScan-PD : For path delay ATPG

TurboScan-BF : For bridging fault ATPG

Other Products from SynTest

TurboBSD : For Boundary-Scan Synthesis

TurboBIST-Memory : For Memory-BIST Synthesis

TurboDFT : For design modifications and integration

TurboCheck : For DFT rule checking

DFT-PRO Plus : A comprehensive package of DFT tools which includes VirtualScan , TurboBSD ,TurboBIST-Memory , TurboDFT , and TurboCheck :

TurboBIST-Logic/Memory : BIST Tool Suite

TurboFault : For Concurrent Fault Simulation

TurboDiagnosis : For scan chains diagnosis

TurboDeskTopDebugger : A desk-top device debugger

OTHER PRODUCTS FROM SYNTEST

TurboFault is a concurrent fault simulator useful where scan/ATPG technology cannot be used or to enhance fault coverage on top of scan/ATPG technology. It is the fastest high capacity concurrent fault simulator based on SynTest's proprietary algorithms in fault simulation technology. With its low memory consumption, user-definable fault detection criteria, fault-tracing, back-tracing and crash recovery capabilities, it combines high performance with versatility and accuracy. It accepts fault lists from most ATPG tools. As input stimuli, it can handle VCD, WGL and Novas FSDB.

TurboDiagnosis and TurboDeskTopDebugger (TDTD) are SynTest's diagnosis tools and desk-top device debugger to be used for physical ICs with scan and/or BIST.

PATENTS

TurboScan