# TurboDFT™

## DESIGN INTEGRATION TOOL SUITE

SYNTEST

*The Testability Company*

Design-for-Test (DFT) tools and methodologies enable automation of many aspects of the semiconductor testing process, ensuring that the chip comes through tape-out and manufacturing on time, according to product specifications and of good quality. DFT tools enable creation of efficient test patterns that detect most major manufacturing defects.

Very complex integrated circuits, known as System-on-a-Chip (SoCs), can be designed in a modular form. Testability circuitry can be inserted into these modules individually. The different modules can then be integrated to create a full chip. Many tasks related to checking and insertion of testability need to be accomplished at a higher level of design abstraction, e.g. register transfer level (RTL), to reduce the complexity one would face working at the gate-level with millions of gates. As part of this methodology, special care needs to be taken to insert and integrate DFT circuits into Hardware Description Language (HDL) codes, right at the RTL stage. To avoid costly surprises before tape-out, all DFT circuits that could result in changes to the designs should be incorporated into the design of each module.

**PRODUCT DESCRIPTION**

TurboDFT™ contains a suite of very useful and powerful general purpose design integration tools. TurboDFT™ allows users to automatically integrate and stitch DFT cores, whether they are created using DFT tools from SynTest or other vendors. Scripts and commands are provided for allowing users to automatically stitch DFT cores with or without boundary-scan control. TurboDFT™ is general purpose because users can also use it to modify and integrate any portion of the circuit throughout complex design hierarchy automatically. TurboDFT™ brings "ease of integration" benefit and eliminates the tedious, error-prone manual stitching process.

Besides the above function, TurboDFT™ can assist users in creating top-level test benches for testing Memory and Logic BIST cores. Users can use the generated test benches to verify each BIST core that may be embedded deep in a hierarchical design.

TurboDFT™ works with SynTest scan (TurboScan™), boundary scan (TurboBSD™), memory and logic BIST (TurboBIST-Memory™, (TurboBIST-Logic™) products to implement SoC level testability schemes enabling comprehensive board/system level tests.

**Benefits of TurboDFT™**

- Automatically integrates and stitches cores with or without DFT in Verilog. Eliminates the tedious, error-prone manual stitching process.
- Supports designs in RTL, Gate-level, or Mixed-level
- Handles stitching of cores throughout various hierarchies
- Automatically generates top-level test benches for Memory and Logic BIST cores with or without boundary-scan control
- Works with most commercially available logic and scan synthesis tools
- Automatically stitches together DFT-ready blocks created by following SynTest DFT products:
  - Scan/ATPG (VirtualScan)
  - Boundary-scan (TurboBSD)
  - Memory BIST (TurboBIST-Memory)
  - Logic BIST (TurboBIST-Logic)
- Implements SoC level testability schemes, enabling comprehensive board/system level tests

**INTRODUCTION**

TurboDFT is a useful and powerful tool for IC design integration and verification. Through TurboDFT, users can integrate embedded BIST circuits (created by SynTest TurboBIST-Memory or TurboBIST-Logic) with chip-top Boundary-Scan circuit (created by SynTest TurboBSD) or without. For those circuits with Boundary-Scan, after the integration, Boundary-Scan instructions can control the BIST logic, reducing the number of I/O pins at chip-top needed to activate the on-chip BIST logic. For those designs without Boundary-Scan logic, TurboDFT can integrate the BIST circuit into the design and generate a top-level test bench for the BIST. Users can use the generated test bench to verify the BIST circuit itself and enable the BIST to test memories or logic.

In most cases, there is a large amount of memory BIST or complex logic BIST modules deeply embedded in a hierarchy of a design, making manual signal connections a laborious and error prone process. TurboDFT references

connection commands issued by SynTest BIST tools, and automatically performs necessary connections.

Not only for DFT, users can generate TurboDFT commands to integrate any portions of the design.

With a wealth of commands, TurboDFT performs necessary circuit modification and integration tasks, throughout design hierarchy, using built-in generic RTL or gate level operations such as signal "cut", "connect", etc.

**Features of TurboDFT™**

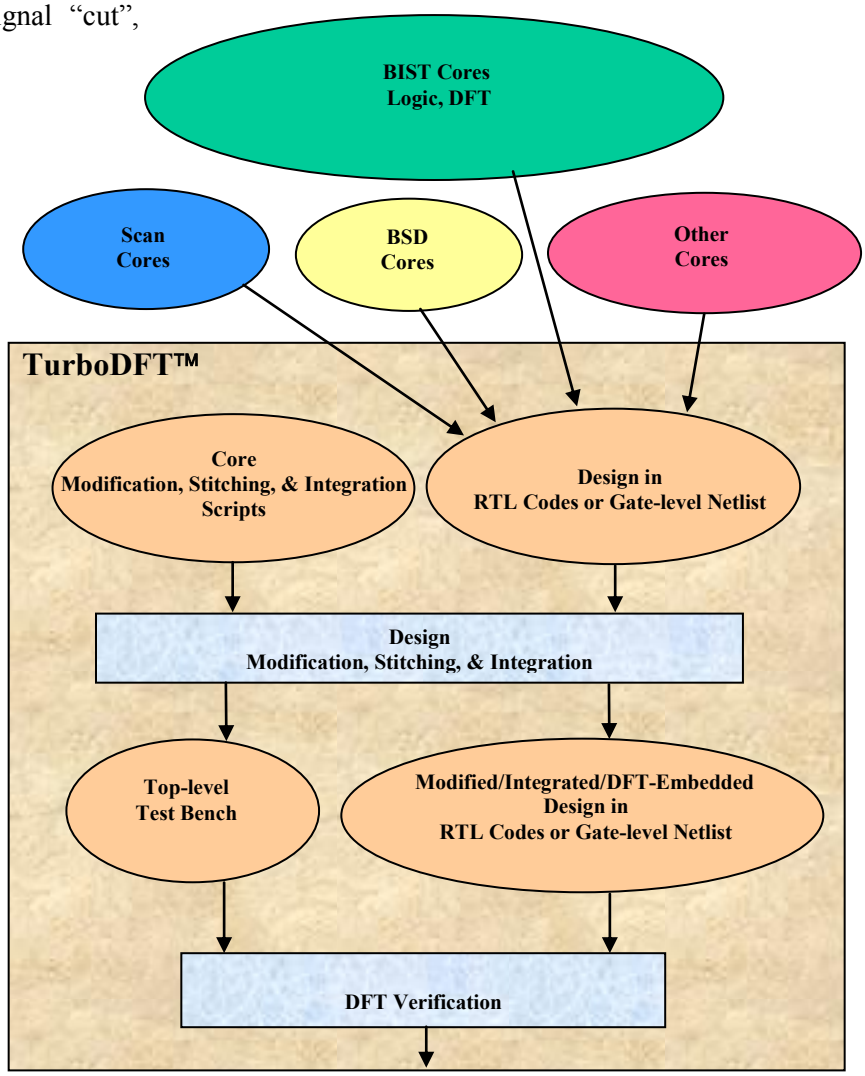
- Accepts RTL and gate level code in Verilog.
- Automatically integrates memory and logic BIST circuits created by SynTest tools with Boundary-Scan, also generates respective chip-top test benches for memoryBIST (TurboBIST-Memory) and Logic BIST (TuboBIST-Logic).
- Automatically integrates the BIST circuit into a design without Boundary-Scan logic and generates a top-level test bench for the BIST.

PLATFORMS

TurboDFT™ runs on Linux platforms and supports Verilog designs either in RTL, gate-level, or mixed-level.

OTHER INFORMATION

To further reduce silicon debug and diagnosis time, TurboDFT™ test benches can be fed into SynTest's TurboDeskTopDebugger™, a low-cost SoC-level DFT prototype debugger.

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