TurboCheck™

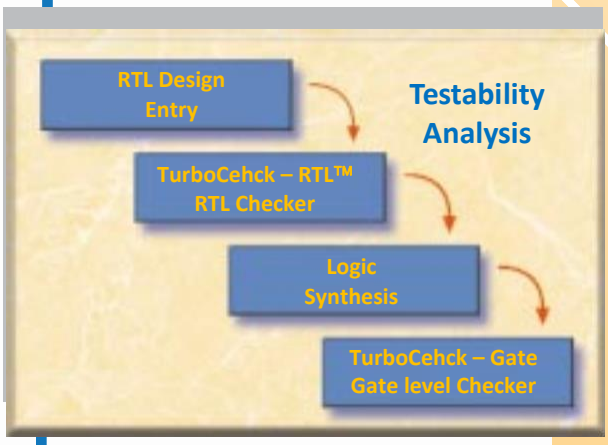
TESTABILITY ANALYSIS TOOLS

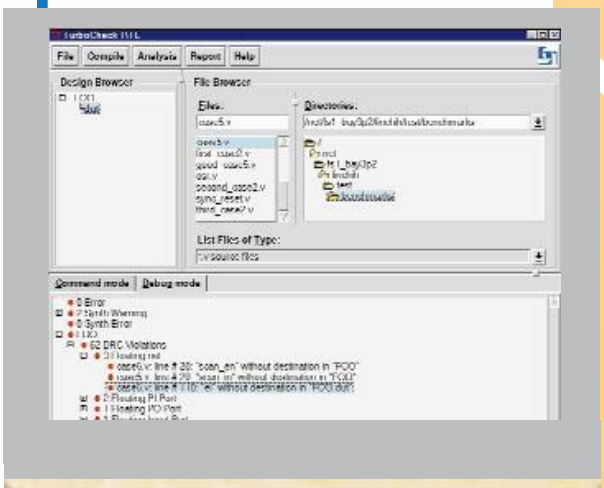
SYNTEST

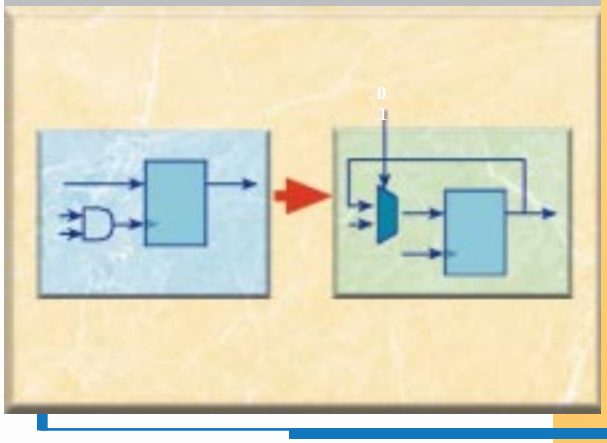
The Testability Company

BENEFITS

- Immediate feedback about potential design and testability problems
- Early detection of testability and synthesis constraint rule violations
- Analyzes RTL and gate level designs
- Provides testability analysis without test vectors
- Guides designers to the best testability solutions
- Selects scan and test points for improved fault coverage







PRODUCT DESCRIPTION

SynTest offers two versions of TurboCheck – TurboCheck-RTL™ and TurboCheck-Gate™ – to support different levels of checking throughout the design cycle. With TurboCheck-RTL, designers can very quickly identify testability problems at the earliest stages of the design cycle, even before the often time-consuming logic synthesis process. With TurboCheck-Gate, designers can perform a structural level check on the final synthesized design to further identify and zero in on any final testability violations that could not be detected at the RTL level. TurboCheck tools compute and report controllability and observability values according to the structure of the design and identify most common – and not so common – testability issues that could prevent efficient ATPG and fault simulation.

PLATFORMS

TurboCheck tools run on Linux platform. TurboCheck-RTL reads synthesizable Verilog RTL and TurboCheck-Gate accepts structural level Verilog.

OTHER INFORMATION

TurboCheck tools find many testability problems quickly and automatically, including floating nets, busses and ports, combinational feedback loops, uncontrollable or unobservable nodes, potential bus contention, combinationally gated clocks, and sequentially generated/gated clocks and asynchronous set/reset conditions. TurboCheck-RTL, in particular, can also be used to identify design coding errors and synthesis constraint violations.

SynTest Service and Support

APPLICATIONS ENGINEERING

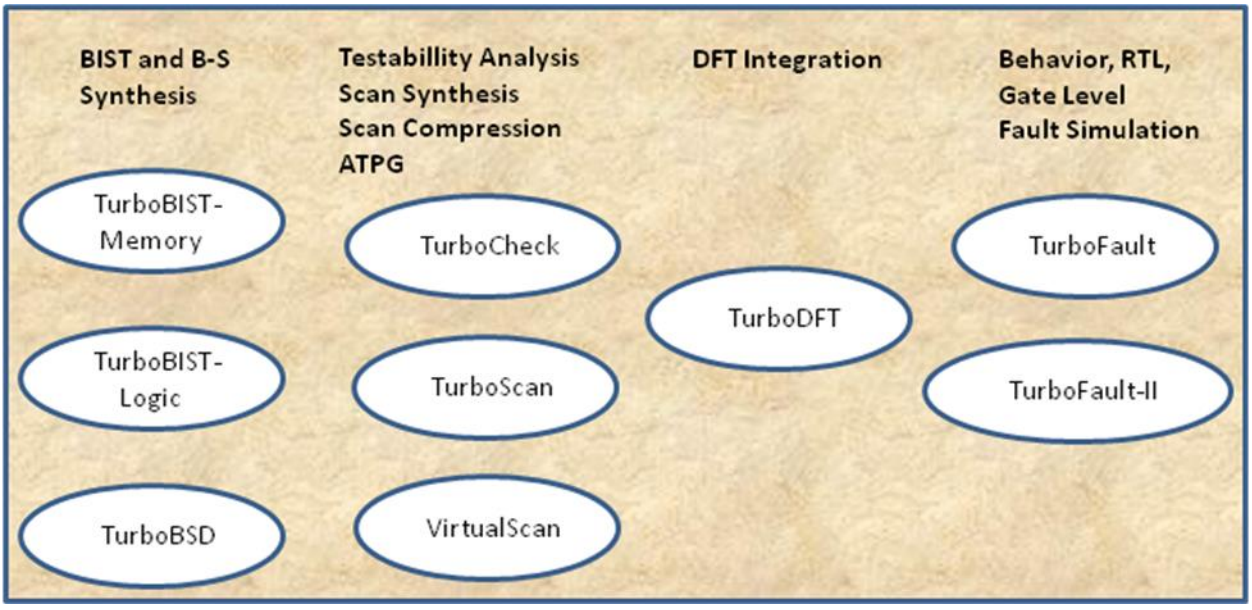
Part of the mission of the Applications Engineering Group is to help our customers to become their own experts in using our tools. Test synthesis is not a 'push button' process. SynTest tools will make the process much easier. Customers who do not have much experience in this area can usually use our help to 'kick-start' their projects. The Applications Engineering group can provide tool and methodology training at the beginning of the design cycle. During tape-out, we are also available to help with any final critical problems related to test synthesis. Our goal is to have our customers feel that they are not alone after they purchase our tools. We are always there to help.

CONSULTING ENGINEERING

In addition to direct product sales, part of SynTest's company mission is to emphasize excellent support for our customers. Our Consulting Engineering Group provides test synthesis and ATPG expertise to our customers who may not have enough resources to accomplish these tasks. We provide a wide range of services starting from design flow methodology integration for our customers. We have expertise in testability analysis, test synthesis, ATPG, and fault simulation. Our past service projects include Pentium class CPUs, advanced 3D Graphics chips, network communication devices, etc. Please contact SynTest for more information on our Consulting Services.

THE SYNTEST PRODUCT FAMILY

The SynTest product family is an ever-growing suite of high quality, advanced tools to help you keep pace with the ever-changing requirements for test design, design for test, ATPG, fault simulation and other state-of-the-art testability solutions. If we do not have it today, we'll partner with you to develop it specifically for your needs.



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