TurboBSD™

BOUNDARY SCAN DESIGN TOOL SUITE

SYNTEST

The Testability Company

The IEEE Standard 1149.1 (Boundary-Scan), proposed by the Joint Test Action Group (JTAG) is a Design-for-Testability (DFT) technique for testing chips and their interconnections on Printed Circuit Boards (PCB). With Boundary-Scan incorporation into IC design circuitry, designers can easily use only few signals to drive the control signals of Built-In Self-Test (BIST) and scan chains. With various instructions in the Boundary-Scan Test Access Port (TAP) controller, PCB designers can also debug signal connectivity among IC chips.

High-speed differential signaling is quickly becoming the preferred approach for moving large volumes of data within and between systems. AC-coupling is used to change the common-mode voltage level when interconnecting different physical layers. In high speed applications, AC-coupling is only recommended for dc-balanced signals. In response to such advanced needs, IEEE1149.6 standard is built on top of IEEE 1149.1, using the Boundary-Scan architecture and the Test Access Port controller.

PRODUCT DESCRIPTION

TurboBSD is a high performance Boundary-Scan design suite that makes Boundary-Scan design a fast and straightforward process. It synthesizes Boundary-Scan cells, the TAP controller and instruction registers. The tool outputs synthesizable Verilog RTL codes that can be customized for users' application and later synthesized using users' target technology libraries.

In addition to the standard IEEE 1149.1 mandatory instructions, TurboBSD also supports custom ID code and private instructions. After synthesis, it extracts the Boundary-Scan chain information from the design and automatically creates corresponding BSDL file. TurboBSD automatically generates implementation and fault model independent functional test sets to verify the integrity of the Boundary-Scan logic implementation. TurboBSD also generates parametric tests (e.g., VOH, VOL, VIH, and VIL) and test patterns to control BIST operations using test information in the Serial Vector File (SVF) format.

TurboBSD is easy to use and reduces BSD time to minutes per design.

Benefits of TurboBSD™

- Automatically synthesizes IEEE 1149.1 as well as 1149.6 compliant Boundary-Scan logic
- Automatically generates (BSDL) (Boundary-Scan description) language file
- Automatically generates Boundary-Scan test patterns, including verification and parametric test benches
- Supports RTL, gate or mixed level netlist generation in Verilog format
- Imports SVF (Serial Vector Format) vector for verification
- Form-based-Boundary-Scan description entry for fast, error free operation
- Reduces Boundary-Scan design time to minutes per design
- Design process independent
- Supports Multiple ASIC vendor technologies
- Has scalable interface mechanism for other Design-for-Test tools

IEEE 1149.6 Specifics

- Provides a set of Boundary-Scan Register AC/DC selection cells and Boundary-Scan Register data cells on AC pins
- Supports the concept of a "test receiver" to input pins that are expected to handle differential and/or AC coupling
- Supports instructions, EXTEST_PULSE, EXTEST_TRAIN, that cause drivers to emit AC waveforms that are processed by the test receivers
- Generates BSDL file containing Advanced I/O description information for the AC ports

USAGE

TurboBSD is used for VLSI chips that require Boundary-Scan logic as defined by the IEEE 1149.1 and/or 1149.6 Boundary-Scan Standard. The distinctive architectural characteristics of this tool are: **** Technology independent synthesis, Boundary-Scan Description Language (BSDL) generation, and test vector creation, * Design process independent synthesis, BSDL extraction, and test vector generation, * Multiple ASIC vendor technology support, * A scalable interface mechanism for other Design-For-Test tools, * Automated verification process, * SVF (Serial Vector Format) vector importing for verification***

TurboBSD reads in a design's primary input and output pins information, inserts Boundary-Scan cells and form a Boundary-Scan chain between core area and IO pins. Also it creates Test Access Port (TAP) controller that generates a IEEE 1149.1 standard conformation state machine to control the Boundary-Scan cells and chain, and mandatory and user-defined private instructions. TurboBSD Boundary-Scan test follows various instructions defined in the IEEE 1149.1 standard architecture. The test also supports advanced multi-TAP System-on-Chip (SOC) design where each embedded core in the SOC has its own TAP.

For designs with high speed differential signals and AC coupling, TurboBSD provides IEEE 1149.6 conforming features - enhanced TAP controller, test receiver insertion, .6 specific instructions, and test pattern generation, etc.

Features of TurboBSD™

- Automatically adds Boundary-Scan cells to the pads and forms a Boundary-Scan chain
- Automatically creates and inserts the TAP controller
- Automatically generates Boundary-Scan Description Language (BSDL) file
- Automatically generates testbench for the Boundary-Scan verification
- Supports test for private instructions using SVF file only
- Supports test strategy for designs with multiple TAP controllers

TurboBSD provides Boundary-Scan capability on IC chips that can benefit both chip designers and Printed Circuit Board designers. Especially, designers may debug entire PCB connectivity or IC chips by using at most five Boundary-Scan signal pins to drive the entire signal pins on the chip.

PLATFORMS

TurboBSD™ runs on Linux platforms and supports Verilog designs either in RTL, gate-level, or mixed-level.

Test Access Port (TAP): The TAP contains four, (optionally five) pins. These signals include Test Clock (TCK) input, Test Mode Select (TMS) input, Test Data Input (TDI), and Test Data Output (TDO), and an optional asynchronously Test Reset Input (TRST).

TAP Controller: The TAP controller is a synchronous finite state machine that controls the instruction and test data registers. The TAP controller uses TMS and TCK signals to transfer states.

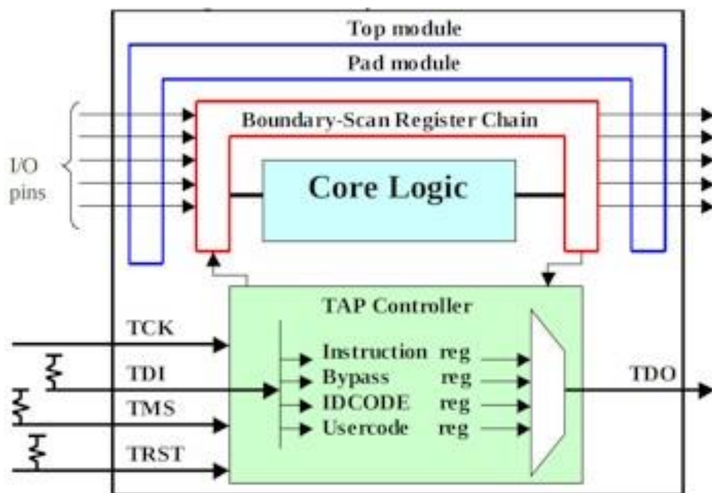
Bypass register: The bypass register is only one bit between TDI and TDO. The path can be selected when no other test data register needs to be accessed during test operation.

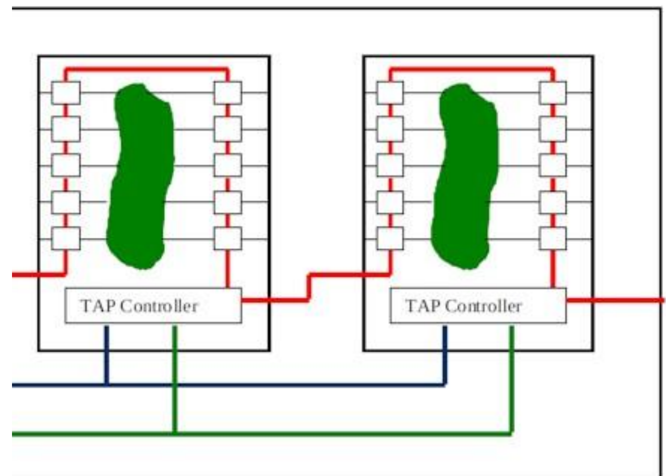
Boundary-Scan register: The Boundary-Scan register is the main test data register, which can be used to test interconnections between ICs under test. The Boundary-Scan register cells will be inserted between core logic and IO pins.

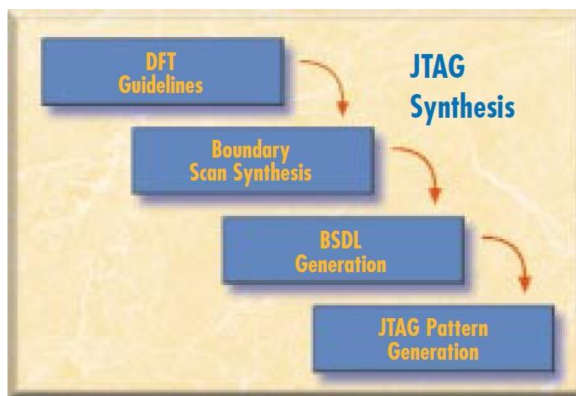
Device Identification Register (Optional): The Device Identification Register contains identification code of the device manufacturer, the part number, and the variant.

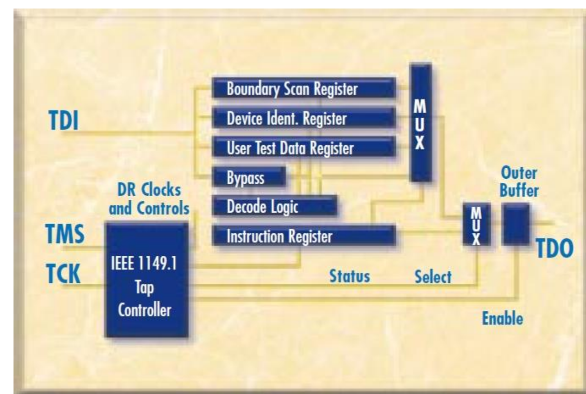
Specific Test Data Register (Optional): This register allows access to design-specific test support features in the core logic, such as self-tests and internal scan paths.

Instruction Register: This register allows either an instruction to be shifted into the design for selecting a test to be performed or a test data register to be accessed, or both.









SynTest Technologies, Inc.
505 S. Pastoria Ave, Suite 101, Sunnyvale, CA 94086
Tel: 408-720-9956   Fax: 408-720-9960

www.syntest.com
info@syntest.com

© 2012 SynTest Technologies, Inc. All trademarks and registered trademarks are the properties of their respective owners