

TurboBIST-Logic™

Tool Suite for Logic BIST



SYNTEST
The Testability Company

Today's SoCs (System-on-Chip) can contain hundreds of memories, several types of logic, dozens of functional blocks obtained from diverse sources, and multiple clocks operating at multiple frequencies. This brings with it a set of challenges in defining a proper test strategy, optimizing test costs and the time required for testing. External access, embedded self-tests and diagnostics go a long way towards helping addressing the test challenge.

It is in this environment that Logic BIST (Built-In Self-Test) makes itself a valuable and an indispensable tool. One of Logic BIST's greatest virtues is its ability to test a circuit at its full operating speed – a capability that even very expensive external automated test equipment (ATE) systems cannot do for super high speed electronics products.

Further, "at-speed" testing, as it is called, has become essential for submicron chips, in which transition delays and other timing faults have become crucial to their operation. Only true clock-rate testing can discover these. Thus, Logic BIST has tackled beyond the familiar stuck-at fault model to transition fault models if timing faults are to be included in the coverage.

The TurboBIST-Logic™ is a powerful, yet easy-to-use tool to incorporate and realize Logic BIST test strategy and logic for complex SoC designs to reduce the cost of manufacture tests and improve the quality by using "at-speed" testing.

It generates BIST architecture for single clock, multiple clock and multiple frequency domains. In these cases the "at-speed" strategy is used in TurboBIST-Logic™. The "at-speed" operation features a patented multi-capture scheme which allows the logic to be tested using "true" clocks; and a fault simulator, which supports stuck-at and transition fault models.

TurboBIST-Logic™ allows users to use a number of strategies for improving fault coverage, such as increasing the number of BIST patterns, re-seeding, adding Test Points, or Top-up ATPG using SynTest's proprietary full scan Automatic Test Pattern Generation (ATPG) tool, TurboScan™.

TurboBIST-Logic™ generates synthesizable RTL blocks as well as script files, which can be used with tools from leading EDA vendors for logic simulation, synthesis and static timing analysis (STA).

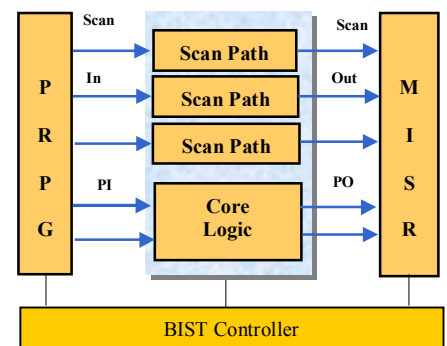
TurboBIST-Logic™ also works with SynTest's Boundary-Scan synthesis tool, TurboBSD™, to implement SoC level testability schemes, enabling comprehensive board / system level tests.

METHODOLOGY AND ARCHITECTURE

TurboBIST-Logic™ is based on the scan method as the fundamental DFT technology. The stimuli originate from a Pseudo-Random Pattern Generator (PRPG) and the test responses are compacted into a Multiple-Input Signature Register (MISR), as shown in the diagram. In case of multiple clock-domain multi-frequency circuits, a pair of PRPG and MISR can be used for each individual clock domain or frequency.

BENEFITS OF LOGIC BIST

- Helps reduce ATE costs during production, by using the IC's built-in "at-speed" testing. Ideal when dealing with SoC designs with multi-million gates/primitives, multiple clock domains, multiple frequencies, and high frequencies.
- Helps improve quality of sub-micron chips, by detecting delay and other timing faults by using "at-speed" testing and a patented multi-capture scheme.
- Helps reduce design time and test costs as well as ensures higher quality and reliability when using multiple instantiation of "legacy" logic circuit blocks or re-using IP cores in different designs.
- Helps in the wafer sorting process and thereby reducing packaging costs.
- Supports in-field remote testing or non-invasive testing of crucial electronic equipment.
- Helps during prototype debug / diagnosis.



Basic Architecture for Logic BIST
PRPG = Pseudo-Random Pattern Generator
MISR = Multiple-Input Signature Register
PI = Primary Input; PO = Primary Output

APPLICATIONS

During Production

- SoC designs with multi-million gates:
The number of patterns generated using Automatic Test Pattern Generation (ATPG) needed to adequately test multi-million primitive designs tends to be very large and applying these large number of patterns takes a very long time on an Automatic Test Equipment (ATE). This could significantly drive up the total test cost for the chip. "At-Speed" Logic BIST offers an alternative solution, which significantly reduces the time required on the testers, driving the chip test cost down.
- SoC designs with high frequencies:
The cost of ATE increases significantly when testing at high speeds is a requirement. Also, appropriate ATE may not be available. Testing high-speed circuit blocks with Logic BIST enables use of low-cost testers to test complex SoCs easing the need for high-speed ATE (which may not be available in the market), and also helping to keep the tester costs down.
- Detecting timing faults:
For sub-micron chips, timing delays and other timing faults become crucial to their operation - especially when clock frequencies are very high. These faults cannot be detected using ATPG test executed at slower speeds. Only "true clock rate" or "at-speed" testing can detect such faults. Logic BIST facilitates such "at-speed" testing and enables detection of transition delay faults and other timing faults. SynTest offers a patented capture scheme for detecting timing faults.
- SoC designs with multiple clocks and multiple frequencies:
For testing circuits with multiple clocks and multiple frequencies, operating the logic at the desired "at-speed" frequency allows for clock-domain crossing fault transfers and hence more comprehensive fault detection.
SynTest offers a patented capture scheme for true multi-clock multi-frequency handling.
- IP cores:
In large SoC designs, it is becoming common to re-use multiple instantiation of "legacy" logic circuit blocks or use IP cores available from many vendors. Overall test creation as well as test execution time for SoC designs can be considerably reduced by implementing Logic BIST for such blocks/cores and then using such "BISTed" blocks/cores in the design.

Such BISTed blocks/cores can also be re-used in subsequent designs, again helping to reduce test cost and to ensure higher quality and reliability.

During Wafer Sort , board, and system test

Simple Go/No-Go self-testing can help in the wafer sorting process and thereby help reducing packaging costs. Similarly such testing can also be used to test the quality of PCBs used in the system.

During Prototype Debug/diagnosis

Scan chains based Logic BIST allows diagnosis of a failing design, pin pointing the pattern where the test fails and then allowing scanning out of the results to identify the failing instances(s).

In the field

Simple Go/No-Go self-testing helps in monitoring the functioning / performance of the SoC. External access is easily provided through the Test Access Port (TAP) via Boundary-Scan (JTAG) link. This is ideal for remote testing or non-invasive testing of crucial electronic equipment.

FEATURES

- Scan based system
- Automatic scan and BIST design rule check and repair
- Optimized PRPG and phase shifter design
- Patented capture scheme for "true" multi-clock, multi-frequency handling
- Minimal clock manipulation
- Fast fault simulation for stuck-at, transition delay faults
- Automatic signature generation using multiple inputs (MISR)
- Mixed-edge flip-flop and gated clock support
- Advanced scan synthesis features, including scan selection, repair, reordering and debug
- Synthesizable RTL code generation for PRPG, MISR, and BIST controller.
- Boundary-Scan (JTAG) interface
- Script files generated for logic simulation, synthesis and static timing analysis (STA) by 3rd party EDA software
- Flexible PI/PO handling.
- Programmable and flexible diagnostic features
- Improve fault coverage through
 - Varying the number of LBIST patterns
 - Efficient clock-domain-based test point insertion
 - Re-seeding of PRPG
 - Top-up ATPG
- Very compact test set generation for top-up ATPG, using SynTest's TurboScan™
- Debug capabilities available through SynTest's TurboDiagnosis™ and TurboDeskTopDebugger™

FLOW

The typical Logic BIST flow as shown in the diagram, starts with a gate-level netlist. As the scan method is the fundamental DFT technology used, the netlist is checked to see whether it has scan inserted into it.

If the netlist has scan already inserted, the first step is to check it for scan design rules. Subsequently, scan extraction is performed.

If there is no scan inserted in the netlist, the first step is to perform scan insertion, which consists of scan selection and scan synthesis and generating a new scanned netlist.

The next step is to configure the Logic BIST, which generates the PRPG, MISR and BIST controller circuits. The users need to define either the number of PRPG patterns or the desired fault coverage in the BIST structure.

These configurations are then checked for BIST rules violations. Subsequently, fault simulation is run and calculations performed to obtain the circuit's logic BIST fault coverage and the final MISR signature.

After running fault simulation, if the circuit's logic BIST fault coverage (F.C.) is not high enough, a number of strategies are available to improve the fault coverage. Each strategy has an impact on logic and/or time that users must study the trade-offs. These strategies are described separately below.

Once the fault coverage reaches a satisfactory level, the Logic BIST RTL is generated along with the script files for design integration. The tool also generates test benches for logic simulation for the BIST logic at RTL or at gate level.

Synthesis and integration

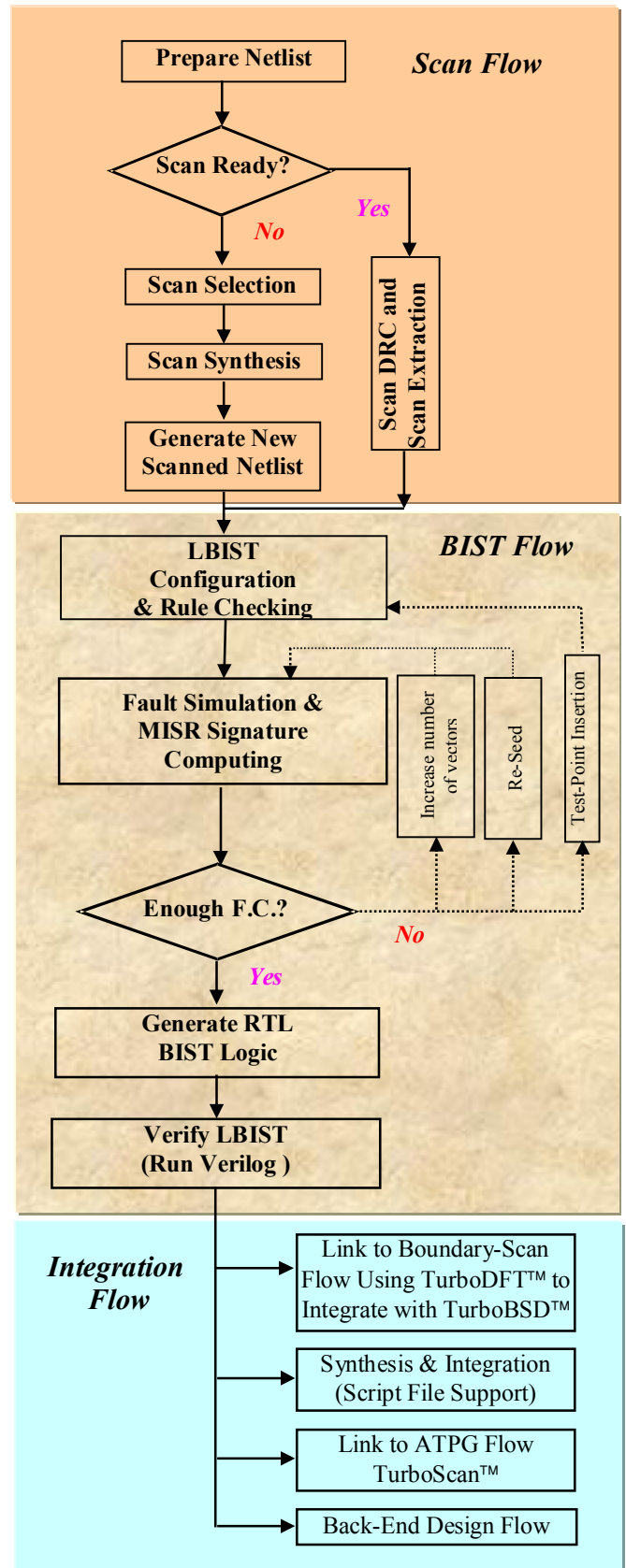
The script files are generated in order to synthesize the design and run the static timing analysis (STA). These script files can be integrated to run the whole chip synthesis and timing check. The script files can be used with tools from leading EDA vendors for logic simulation, synthesis and static timing analysis (STA).

By linking to a Boundary-Scan flow, via TurboBSD™, users can simply use the TAP controller to drive the LBIST operation. The program generates the serial vector format .svf and guides TurboBSD™ to link the necessary signals to the interface of LBIST.

After integration, users will enter back-end design flow. If an ECO requires combinational logic change, users simply rerun simulation to get a corresponding golden signature. If an ECO requires a flop-flop change, the logic BIST control logic has mechanism to support varying length scan chain(s); therefore, there is no need to re-run the tool.

“TRUE CLOCKS”

If a circuit has three clocks, e.g., 150MHz, 100Mhz and 66Mhz, TurboBIST-Logic™ will test the circuit at these three exact frequencies, and not at 150MHz, 75MHz and 37.5MHz, using the divide-by-two approach employed by other Logic BIST tools.



Strategies for Improving Fault Coverage

Each strategy obviously has an impact on the “total test time,” “timing overhead of the design,” “area overhead,” and “overall improvement in fault coverage”. Users need to consider the trade-offs before selecting one or a combination of these strategies to suit their overall requirements.

- **Increasing the number of BIST patterns:**

If users set a pattern number, but it cannot achieve the expected fault coverage, users can increase the number of patterns in the LBIST configuration program and re-run fault simulation to get a new signature with respect to the new pattern set.

- **Adding Test Points:**

If the fault coverage is not at desired level with PRPG patterns alone, TurboBIST-Logic™ can add test points to increase the fault coverage. The test points can be control points or observe points. The tool has default test point designs. Users can also supply their own test point designs.

- **Re-seeding:**

Multiple seeds for the PRPG can be shifted through the JTAG ports. There is no need for extra hardware and timing overhead. A potential benefit is getting higher fault coverage by selecting effective seed numbers.

- **Top-up ATPG:**

To further increase overall fault coverage, TurboBIST-Logic™ works in tandem with SynTest’s proprietary full-scan ATPG tool, TurboScan-ATPG. As a result users will be able to run the Top-up ATPG, for these faults not detected by the PRPG patterns and/or test point patterns, to increase the overall fault coverage. This hybrid methodology overcomes the basic drawback of ATPG requiring a long run time, as now only a relatively small number of faults are still to be detected.

Solutions for Diagnosis and Device Debug

Two tools supporting diagnosis and debug as follows.

Features of TurboDiagnosis™

- Analyzes ATE or a debugger’s device failure log
- For TurboBIST-Logic, checks for integrity of PRPG/MISR and logic BIST controller
- Identifies failed scan chain(s), scan chain segment(s), and, ultimately, a single failed flip-flop.
- Analyzes the combinational logic cone feeding the failed flip-flop and identifies possible root causes. The result is a list of possible suspects (gate, signals within the logic cone) with their respective probabilities of being the actual root cause(s).

Features of TurboDeskTopDebug™

- A desk-top IC debugger containing a small JTAG (Boundary-Scan) based hardware unit with an USB interface, connecting to users’ PC as a host (containing design/DFT/device failure information and debugger software), and to a users’ circuit board where the failed physical device resides.

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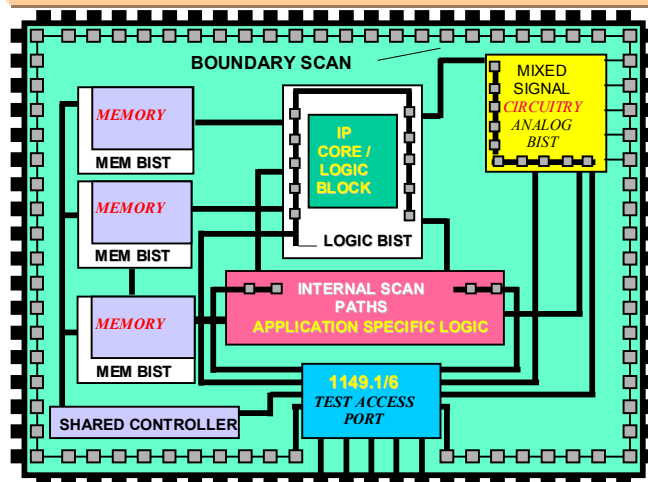
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LINK TO BOUNDARY-SCAN (JTAG) FLOW

To implement SoC level testability schemes, enabling comprehensive board/system level tests, TurboBIST-Logic™ works with SynTest’s Boundary-Scan Synthesis tool, TurboBSD™. By using TurboDFT™ to integrate the two DFT strategies, users can use the TAP controller to drive the Logic BIST operation. The tool generates the serial vector format .svf and links signals between TurboBSD™ and TurboBIST-Logic™.



ORDERING INFORMATION

- **TurboBIST-Logic™- Logic BIST Tool Suite Options**

- TurboScan™: For Top-up ATPG
- ATE Test Program Outputs
- TurboBSD™: For Boundary-Scan Synthesis
- TurboDiagnosis™/TurboDeskTopDebugger™: For Logic BIST Debugging and Diagnosis

- **Other products from SynTest**

- TurboCheck™: For DFT Rule Checking
- TurboScan™-Synthesis: For Scan Synthesis
- TurboBIST-Memory™: For Memory-BIST Synthesis
- TurboDFT™: For design modification and integration
- TurboFault™: For Concurrent Fault Simulation

PATENTS

SynTest products are protected by

U.S. Patents: 6,954,887; 6,957,403; 7,007,213; 7,032,148; 7,058,869; 7,124,342; 7,191,373; 7,210,082; 7,228,479; 7,231,570; 7,260,756; 7,284,175; 7,331,032; 7,412,637; 7,412,672; 7,434,126; 7,444,567; 7,451,371; 7,512,851; 7,552,373; 7,590,905; 7,721,172; 7,721,173; 7,735,049; 7,747,920; 7,779,322; 7,779,323; 7,783,940; 7,904,773; 7,904,857; 7,925,947; 7,945,830; 7,945,833; 7,996,741; 8,091,002; 8,161,441; 8,219,945.

European Patents (Registered in the United Kingdom, France, and Germany): 1,360,513; 1,364,436; 1,370,880; 1,377,981.

Japan Patents: 4301813; 4733191; 4903365.

China Patent: ZL02804862.1.

TurboBIST-Logic™