TurboFault™

A Concurrent Fault Simulator

SYNTEST
The Testability Company

Today, integrated chips with multi-million gates, containing logic, memory and IP Blocks are becoming commonplace. At the same time, controlling costs and maintaining high quality standards are critical to the success of any such development. Fault grading is an accepted method for measuring manufacturing quality. Fault simulation plays an important role in providing accurate fault coverage estimate for functional patterns used for test. It also provides a lower cost alternative for off-line debugging of production faults.

Fault simulation can compliment Scan/LBIST test by selecting functional patterns to improve fault coverage. Fault coverage for custom cells unfriendly to DFT or IP blocks provided by external vendors can only be measured with Fault simulation.

High Performance Fault Simulation

TurboFault™ combines high performance, versatility and accuracy for classical test fault grading. **TurboFault™** is the fastest concurrent fault simulator based on the latest advances in cycle-based simulation technology. It simulates even faster than expensive hardware-accelerated fault simulators. **TurboFault™** supports synchronous and asynchronous designs at the gate level, including tri-state gates, latches, flip-flops, single/multi-port RAMs, complex bus resolution functions, and User Defined Primitives (UDPs). It reads Verilog or VHDL gate-level netlists, STIL, WGL patterns, VCD/eVCD files as well as Standard Delay Format (SDF) timing files.

Advanced Cached-Concurrent™ Algorithm

TurboFault™ utilizes proprietary algorithm optimized for modern computer hardware that maximizes the power of today's workstations. SynTest Cached-Concurrent™ algorithm with the new Fast Queue™ technology combines the best of unit delay and cycle-based capabilities. The Cached-Concurrent™ operation reduces the number of gate evaluations; Fast Queue™ manages fault lists efficiently

TurboFault™ makes fault simulation an integral design tool for generating a manufacturing test set of high quality. TurboFault™ supports single timing delay for simulation accuracy and flexibility, without sacrificing speed.

TurboFault™ reports faults as Hard Detect, Probable Detect, Potential Detect, Undetected, Hyperactive, Oscillatory, or Uncompleted. Any or all of these can be combined in single or multiple reports which can be “wrapped around” as inputs for the next incremental fault simulation run, or passed to spreadsheet or plotting tools for analysis.

Low memory consumption

Because fault simulation can consume memory very quickly, memory management is critical. TurboFault™ handles this by combining very efficient memory management, with special fault handling capability resulting in low memory consumption.

Features of TurboFault™

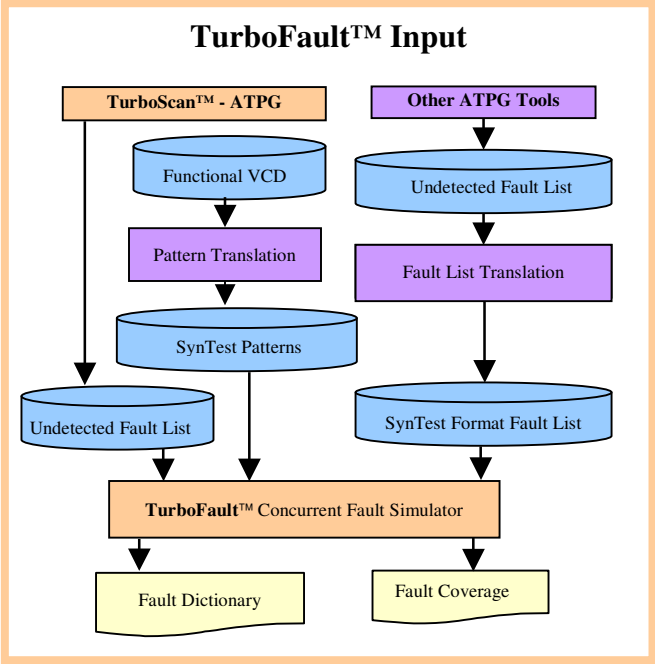
- Supports Stuck-at 0/1, Bridging and Transition Delay Fault Models.
- Supports toggle tests and Iddq tests.
- Uses cycle-based simulation technology.
- Advanced Cached-Concurrent™ Algorithm with Fast Queue™ technique for Low memory consumption.
- User Definable Fault Detection Criteria.
- Fault Tracing Capability.
- Offers Multi-Pass, Incremental Simulation, Distributed Processing and Crash Recovery Capability.
- Accepts undetected faults from SynTest TurboScan™ and other ATPG tools.
- Offers a variety of reports/outputs, such as histograms, aggregated fault coverage reports, module level fault coverage reports; recommends list of patterns and a list of cut-off points.
- Built in back tracing capability and forward/backward tracing links to Debussy.
- Fast node configuration mode for simulating massive FPGA designs.
- Checkpoint/restore function to shorten the fault simulation time.
- Parallel scan pattern support for fast verification of ATPG patterns.

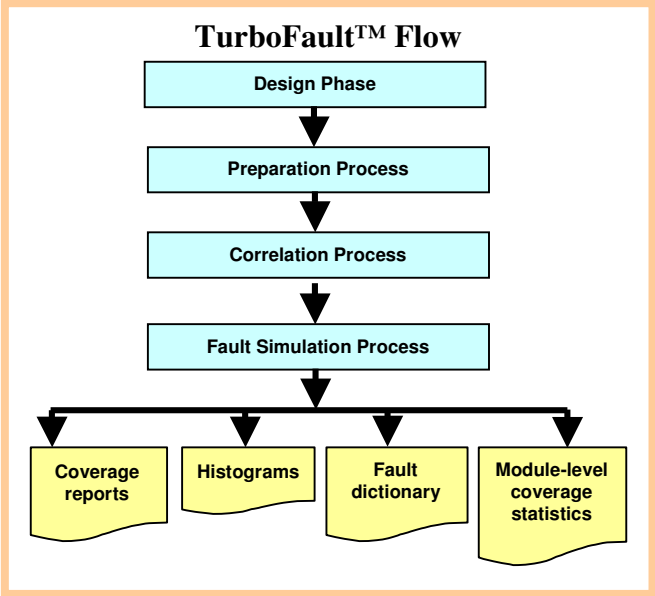
Why Fault Simulation:

- To measure fault detection coverage in designs where DFT schemes are not used due to the concerns related to area overhead, which would be added to the circuit, if DFT were to be used.
- To measure fault coverage in areas not observable by scan or BIST structures, or where complete and reliable accuracy is required.
- To measure fault coverage and estimate defect detection levels in BIST algorithms.
- To select additional patterns to test parts of design not covered by the existing test patterns, or to understand and correct fault coverage problems.
- When using multiple instantiation of “legacy” logic circuit blocks or re-using IP cores in different designs, to check that the various embedded blocks and their vectors have been correctly glued together with the rest of the chip to produce a complete set of test vectors and a test program.
- Low cost alternative
  a) To develop test-generation software. Many designers still create test programs manually and then grade the test vectors using fault simulation.
  b) To use a production tester to debug a production test. With a fault simulator this can be done off line.

Inputs to TurboFault™

- Gate-level cell library files in Verilog or VHDL, gate-level or transistor-level cell netlists
- Analog circuits - PLL, Memory and CAM may be in behavioral level
- SDF timing back-annotation file (if available).
- Test Patterns in VCD/eVCD, STIL, WGL, or FSDB (Debussy)
- Fault list/coverage report: Output from an Automatic Test Pattern Generator (if available)
- TurboFault™ can read in reports from SynTest TurboScan, Synopsys TetraMax and Mentor Fastscan tools, as well as from ZyCAD





Protection for "run-away" simulation runs

TurboFault™ provides special handling for Oscillating and Hyperactive faults. Oscillating faults are handled using a window timer approach. Any faults that oscillate longer than the "window" time are considered oscillating and automatically dropped. Hyperactive faults are also detected internally and optionally dropped.

User Definable Fault Detection Criteria

TurboFault™ allows a user to define the criteria for a fault in order for it to be declared as detected. This gives the simulator the highest flexibility to emulate many test environments and Automated Test Equipment.

Debugging using Back Trace Capability

There are several options for Debugging in TurboFault™. The popular ones among them are built-in back tracing capability and forward/backward tracing capability by using links to Debussy. Internal nodes dumped using either VCD or FSBD format.

Crash Recovery Capability

TurboFault™ not only provides first-rate performance but also power with second-to-none reliability. The crash recovery function allows recovery of the simulation data and protects results from any environmental adversities, such as network glitches and power outages. This feature ensures the highest and fastest rewards from the investment of time and computation resources.

Multi-Pass and Incremental Simulation

TurboFault™ is intelligent enough to inspect the computer resources available and determine the optimal configuration for running a fault simulation job. TurboFault™ can partition the faults into groups and submit simulation tasks in multiple passes for each group. This automatic partitioning capability optimizes the number of faults per pass and thus reduces paging. The results from different groups are then automatically merged in the final report.

A stimulus suite often consists of test pattern files where each pattern file requires a separate fault simulation session. Incremental simulation reduces the number of patterns per run. TurboFault™ provides an easy way to accumulate fault grading results from different fault simulation sessions, avoids a tedious and time consuming effort of merge, and thus frees the user to focus on analyzing the overall result.

User Interface & Library Modeling

TurboFault™ uses the powerful Tcl (Tool Command Language) user interface making fault simulation control easier and more intuitive. Fault simulation control can be quickly implemented in Tcl scripts. The Tcl interface supports both batch and interactive modes.

TurboFault™ accepts gate-level cell descriptions, User Defined Primitives (UDPs) and also provides a cell library builder to build gate-level models. The library is compatible across all SynTest tools, including ATPG. TurboFault™ supports Verilog and VHDL gate-level and single timing models.

TurboFault™ memory modeling utility provides basic memory building blocks for handling ROMs, and single as well as multi-port RAMs, either synchronous or asynchronous. SynTest model generators support common memory model vendors, e.g. ARM, Virage Logic et al.

Stuck-at Fault Support

Short and open defects usually cause the signal net or line to remain at a fixed voltage level. The corresponding logical fault models supported by **TurboFault™** is of a signal Stuck-at-0 (SA0) or Stuck-at-1 (SA1).

Bridging Fault Support

TurboFault™ supports bridging faults model. The types of bridging fault models supported are, wired-x, wired-or, wired-and, force-0, force-1 and dominate faults. The fault list for the bridging fault is to be provided by the designer from the layout data. For bridging fault simulation TurboFault switches to its bridging fault engine, and other setup is very similar to the stuck-at fault simulation flow.

Transition Fault Support

TurboFault™ also supports transition fault model in addition to the stuck-at and bridging fault models. Transition fault models of slow-to-rise and slow-to-fall are supported. The transition delay time has to be carefully specified by the designer and the simulation is run with the transition fault engine. The designer can supply the fault list for Transition fault simulation. Or it can alternately be generated from the collapsed fault list provided by the TurboFault programs. The rest of the flow is very similar to the stuck-at fault simulation. **TurboFault™** provides support for popular third party fault lists. During fault collapsing phase, a collapsed fault list is created for use with the Transition Fault simulation built-in engine. Each node can have both slow-to-rise/fall transition faults.

IDDQ Testing

If users want to increase the coverage for the stuck-at simulation, then IDDQ testing is a popular solution. **TurboFault™** is capable of doing IDDQ simulation and will identify the number of desired test points for the IDDQ testing. TurboFault will then use IDDQ engine during simulation to give the additional coverage information and list of test points. The flow is very similar to normal stuck-at simulation.

Reporting

TurboFault™ produces concise yet detailed reports on fault coverage, fault classifications, module level statistics and toggle tests. It reports faults as Hyperactive, Hypertrophy, Oscillatory, Hard Detect, Probably/Potentially detected, Undetected, or Uncompleted. Any or all of these can be combined in single or multiple reports which can be “wrapped around” as inputs for the next incremental fault simulation run, or passed to spreadsheet or plotting tools for analysis.

In addition, undetected faults can be passed directly to SynTest ATPG tools for additional processing.

TurboFault™ Outputs

- A histogram that gives fault coverage changes along the time line for each pattern file.
- An aggregated fault coverage report that gives status of each potential defect/fault along with pins and patterns that detect the fault can be reported as well.
- Module level fault coverage reports: Give the coverage numbers for each individual module
- Module level toggle test reports

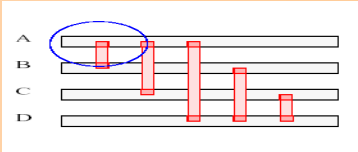
Bridging Fault Support

Source

- Bridging Faults usually come as pair of nodes which are adjacent from the layout data
- Supplied by the designer

Types Supported

- Wired-X, -Or, -And
- Force-1, -0
- Dominate-1, -0



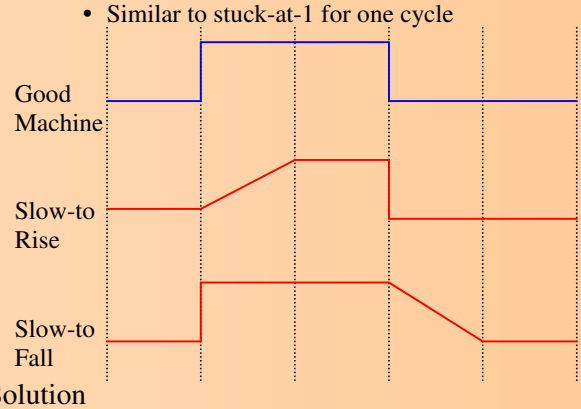
Fault List Formats

Fault list conversion scripts

Transition Fault Support

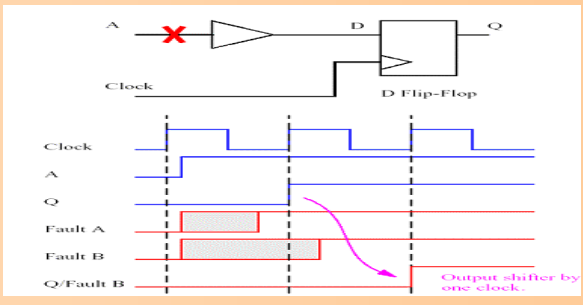
Problem

- Gate Delay reaches to a point where the transition does not reach the output before the end of the clock even along the shortest path
  - Slow to rise
    - Similar to stuck-at-0 for one cycle
  - Slow to Fall
    - Similar to stuck-at-1 for one cycle



Solution

- Choose the right Transition Faults
  - For single clock domain, the transition fault delay time has to be longer than the clock cycle time
  - For Multiple clock cycle domain
    - The transition fault delay could be that of the longest clock cycle
    - Transition Fault coverage could be calculated per clock domain



Broadside Load of ATPG scan pattern

TurboFault has the capability to do broadside loading which makes it very easy to verify the coverage numbers that ATPG reports. Chip vendors who want to correctly verify the accuracy of the ATPG numbers now do so by easily running those scan patterns in TurboFault. ATPG Patterns for both stuck-at and transition fault coverage are possible for verification in TurboFault environment.

TurboFault™ – The Unique Fault Simulator

The mission of a fault simulator is to measure the quality of test patterns for detecting possible defects introduced in the chip manufacturing process.

The patterns are simulated by applying them to the design while injecting a "fault model" of a specific known manufacturing defect. If an erroneous output can be observed on the primary ports of the chip, it will be safe to assume that the defect will be detected by the same patterns in the real manufacturing test.

For millions of possible defects, there will be millions of logic simulation tasks to complete. To reduce this computation cost, many solutions have been proposed in the past 30 years. Their main focus has been on how to identify the redundancy among the millions of logic simulations and how to eliminate it.

Two approaches are widely adopted today:
- The concurrent simulation algorithm
- The differential simulation algorithm

The concurrent simulation approach is believed to provide the most accurate results with full timing support. However, it falls short on the overall performance and memory consumption.

The differential simulation algorithm is able to handle very well combinational circuits but the overhead to deal with sequential logics may offset any performance advantage. Its application is often limited to pure synchronous designs while the concurrent algorithm is far more versatile in handling both types of designs.

TurboFault™ is based a on brand-new fault simulation algorithm, which is basically a combination of concurrent and differential approaches.

Unique kernel implementation in TurboFault™ of such hybrid technique allows it to keep the accuracy, flexibility and circuit compatibility of the concurrent algorithm, while the application of the unique differential algorithm helps it to reduce the memory usage and improve the overall performance.

At the same time, a very fast gate level logic simulation engine gives TurboFault™ a solid base to boost.

Optimizing Fault Simulation Time

For huge designs, initialization stimulus could take long before the actual simulation is run. e.g. in FPGAs a lot of time is used in the configuration and the actual time for simulation may be very short. Fast node configuration could be employed to shorten the simulation time here. Some large ASIC designs may need lot of memory data and initialization of internal nodes. Using functions like Checkpoint /Restore, users could save a lot of time for Fault Simulation.

Distributed Processing

TurboFault™'s distributed processing capability enables it to break the overall fault simulation task into multiple smaller tasks, assign these jobs dynamically to various machines available on the local network and collect/collate results. If one machine fails, jobs will automatically re-assigned to other available machine.

Ordering Information

Licensing

To enable users fully utilize concurrent simulation capabilities, SynTest offers TurboFault™ licenses as "Main" licenses and "Peak" licenses.

The Peak licenses can be procured for short-term durations, in license month units, after a main license is procured, to help run fault grading on multiple machines.

The ability of TurboFault™ to run on networked PCs with Linux OS, offers a low-cost solution for fault grading projects.

Other Products from SynTest

TurboScan™, **VirtualScan**™, **UltraScan**™: For Scan Synthesis and ATPG for stuck-at faults. Plus select test program formatter for one ATE.
TurboBSD™: For Boundary-scan Synthesis
TurboBIST-Logic ™: Logic BIST SynthesisTool Suite
TurboBIST-Memory™: For Memory-BIST Synthesis
TurboDFT™: For DFT Integration
TurboCheck™: For DFT Rule Checking
DFT PRO Plus™: A comprehensive package of DFT tools which includes TurboScan™, TurboBSD™, TurboBIST-Memory™, **TurboDFT**™: and TurboCheck™:
TurboFault™: For Concurrent Fault Simulation
TurboDiagnosis™: For scan chains diagnosis

Platforms

TurboScan™ runs on Sun Solaris, HP-UX and networked Linux operating PCs.

SynTest is now offering Solutions For Diagnosis and Failure Analysis of Scan Chains and Logic BIST with a set of products as follows:
TurboDiagnosis-Scan™, **TurboDiagnosis-VScan™** and **TurboDiagnosis-LogicBIST™**.

SynTest is also offering Solutions For Diagnosis and Failure Analysis of embedded memories using SynTest Memory BIST product. Reports failed address and/or bits each cycle when in the diagnosis mode:
TurboDiagnosis-MemoryBIST™.

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