SynTest Proprietary Technology for At-Speed Testing and Test Compression

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Logic BIST Architecture

- Original Clocks: CK1, CK2
- Start, Finish, Result
- TDI, TDO, TCK, TMS
- Controller
  - Clock Gating Block: CCK1, CCK2
  - Clock Domain #1
    - TPG: PRPG1, PS1/SpE1
    - Input Selector
    - Clock Domain #2
      - TPG: PRPG2, PS2/SpE2
      - BIST-Ready Core
      - ORA: MISR1, MISR2
      - PO/PO: Original Outputs
      - PI/SI: Original Inputs

Additional notes:
- TCK1, TCK2, CCK1, CCK2
- Original Inputs: PI/SI
- Original Outputs: PO/SO

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**Test Timing Control - 1**

**Staggered Double-Capture (SynTest Patent)**

- Detect stuck-at & delay faults (clock domain #1).
- Detect stuck-at & delay faults (clock domain #2).
- Detect stuck-at faults (clock domain #1 → clock domain #2)
- Detect delay faults (clock domain #1 → clock domain #2) for proper \( d \).
- Need only one single and slow SE signal.
- True at-speed testing when there are unrelated clock frequencies.
Test Timing Control - 2

Staggered Skewed-Load (SynTest Patent)

- Detect stuck-at & delay faults (clock domain #1).
- Detect stuck-at & delay faults (clock domain #2).
- Detect stuck-at faults (clock domain #1 → clock domain #2)
- Require multiple at-speed SE signals.
- True at-speed testing when there are unrelated clock frequencies.
Comparison

Capture Aligned Skewed-Load
Launch Aligned Skewed-Load

Staggered Skewed-Load

Staggered Double-Capture

Control Complexity
Over-Test

high
low

easy
Physical Implementation
difficult
VirtualScan Architecture
(SynTest Patent)

ATE
Test Responses

Expected Responses

Test Patterns

Pass/Fail

VirtualScan Inputs

VirtualScan Circuit

Full-Scan Circuit

Broadcasters

Compactor

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UltraScan Architecture
(SynTest Patent)
Soft Errors

- **Logic soft errors**
  - Flip-flops
  - Latches
  - Combinational Logic

- **Memory soft errors**
  - Considered a solved problem
  - Using ECC

Soft-Error Rate Distribution
Source: IEEE Computer [Mitra 2005]
Robust CSER Cells

• **Concurrent Soft-Error Resilience (CSER)**
  - Soft-error resilience (DFR)
  - Slow-speed snapshot (DFD)
  - Manufacturing test (DFT)
  - Slow-speed signature analysis (DFD)
  - Defect tolerance (DFR)

• **Robust CSER Cell**
  - Uses DFT, DFD, and DFR techniques
  - Can be regarded as a design-for-excellence (DFX) cell
Conclusions

• Transition from a Tool vendor to a DFT IP provider
  - to partner with end users
  - to partner with EDA, library, and IP vendors
  - to partner with ATE and design service houses

• Business Model
  - Licenses DFT/DFD patents & architectures for annual fee
  - Per design fee for using test compression or logic BIST IP

• Training and consulting services when requested

• The DFT textbook (808 pages) published by Elsevier in July 2006 entitled *VLSI Test Principles and Architectures*

• The DFX textbook (896 pages) published by Elsevier in November 2007 entitled *System-on-Chip Test Architectures*

• The EDA textbook to be published by Elsevier in Dec. 2008 entitled *Electronic Design Automation: Synthesis, Verification, and Test*