DFT–PRO *Plus*™

SYNTEST

The Testability Company

Design-for-Test (DFT) tools and methodologies enable automation of many aspects of the semiconductor testing process, ensuring that the chip comes through tape-out and manufacturing on time, according to product specifications, and of good quality. DFT tools enable creation of efficient test patterns that detect most major manufacturing defects.

Very complex integrated circuits, known as System-on-a-Chip (SoCs), can be designed in a modular form. Testability circuitry can be inserted into these modules individually. The different modules can then be integrated to create a full chip. Many tasks related to checking and insertion of testability need to be accomplished at a higher level of design abstraction, e.g. register transfer level (RTL), to reduce the complexity one would face working at the gate-level with millions of gates. As part of this methodology, special care needs to be taken to insert DFT circuits into the Hardware Description Language (HDL) codes, right at the RTL stage. To avoid costly surprises before tape-out, all DFT circuits that could result in changes to the designs should be incorporated into the design of each module at an early stage of design.

DFT-PRO *Plus*™ offers a comprehensive DFT solution covering gate-level scan synthesis and ATPG, memory Built-In Self-Test (BIST) synthesis and Boundary-Scan design (BSD) synthesis. The corresponding tools generate RTL blocks that fit seamlessly into an existing synthesis flow. This gives the user the freedom to choose any commercially available logic and scan synthesis tools from vendors like Cadence, Incentia, Mentor, or Synopsys and enables a one-pass RTL to GDSII synthesis flow. It also eases overall design floor planning.

Tools for checking DFT rule violations, and integrating various DFT blocks and design RTL codes are also included in the package. The testability checker conducts an extensive DFT rules check at RTL. This alleviates the tedious manual checking and coding at RTL. It also offers automatic DFT rule checks and repair at gate-level, after synthesis.

VirtualScan™, included in the package, is a tool suite for VirtualScan synthesis and ATPG, using SynTest's patented VirtualScan™ technology. It helps companies that develop million-gate SoCs to expedite their product development through the test process, and achieve a 10x to 100x reduction in the cost of semiconductor testing. It generates XtremeCompact™ test vectors, which reduce the test data volumes and test cycle volumes. Thus, this reduces the need to upgrade to more expensive, next generation Automatic Test Equipment (ATE) or expand existing ATE scan pattern memory. It offers high fault coverage test patterns and a smooth migration into an existing scan ATPG flow.

DFT–PRO *PLUS*™

Integrated DFT solution for VirtualScan synthesis and ATPG, memory BIST synthesis and Boundary-Scan synthesis

BENEFITS:

- Generates DFT blocks at RTL
  - Eases logic synthesis* and design floorplanning
- Checks DFT violations at RTL
  - Averts time-consuming and costly post-synthesis changes
  - Auto-repair capability available
- Generates XtremeCompact™ scan patterns using VirtualScan™ technology
  - Smaller test data volume and shorter test time
  - Reduces cost of semiconductor testing – 10x to 100x
  - Extends life of existing ATE for large SoC designs
- High fault coverage
- Smooth migration into existing scan ATPG flow

* Works with commercially available logic and scan synthesis tools from vendors like Cadence, Incentia, Mentor, or Synopsys.

DFT-PRO *PLUS*™

Tool suite for
- VirtualScan synthesis at RTL
- Boundary-Scan synthesis at RTL
- Memory BIST synthesis at RTL
- DFT integration
- DFT rule checking and violation repair
- Scan chain extraction or stitching
- VirtualScan ATPG
- ATE test program outputs

With VirtualScan™, an extremely large number of short scan chains within the SoC can be virtually accessed from outside the chip with a limited number of pins assigned as scan pins. Inside the chip, SynTest's patented circuitry is used to broadcast each external scan-input chain to a user-selectable number of internal scan chains using a broadcaster and, at the other end, compact them into the original number of external scan chains, using a compactor. The number of internal scan chains for each external scan chain is called the "Split Ratio". It is user-selectable.

VirtualScan Synthesis

Based on the Split Ratio selected, the broadcaster and compactor circuits are generated as RTL blocks. The area impact of the broadcaster and compactor is predictable and extremely small.

These RTL blocks are then synthesized along with the design RTL codes and other DFT RTL blocks into a gate-level netlist. As the DFT blocks are at RTL, it eases the overall design floorplanning decisions carried out at the RTL stage.

VirtualScan™ also contains tools for scan synthesis at gate-level for users who prefer to use SynTest's scan synthesis tools. This process is performed after the RTL codes have been synthesized into a gate-level netlist. It provides scan selection based on clock domains and the scan flip-flop count. It automatically repairs testability violations, when requested.

SynTest recommends running the scan-inserted gate-level netlist through TurboCheck-Gate™ to check the design after it is synthesized into gates. It can perform a structural-level check on the final design to identify and zero-in on the final testability rule violations.

Subsequently, scan extraction, and scan stitching if required, is performed on the scan-inserted gate-level netlist and the scan data fed to the VirtualScan ATPG.

Benefits of VirtualScan™

- Reduces cost of semiconductor testing – 10x to 100x
- Extends life of existing ATE for large SoC designs
- Smaller test data volume and shorter test time
- Short test development time with no iterations
- High fault coverage
- Predictable and very low hardware overhead
- Smooth migration into existing scan ATPG flow

Virtual Scan Architecture

Split Ratio = Number of internal scan chains for each external scan chain
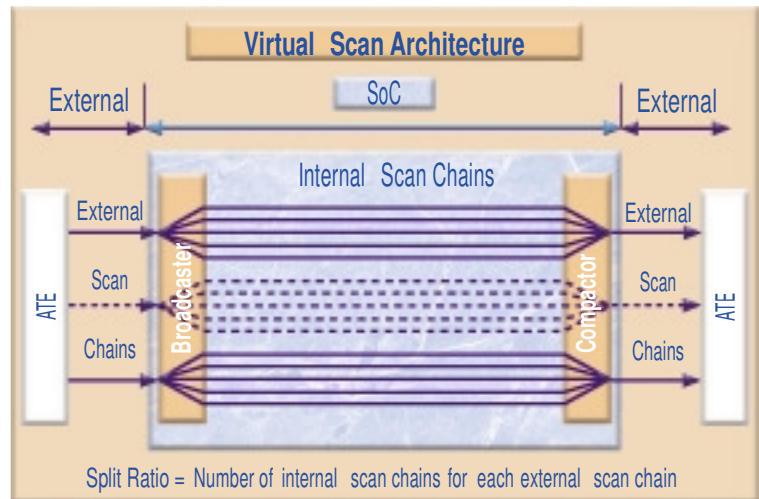
Memory BIST

Many of today's chips demand more embedded memories than ever before, comprising of SRAM, ROM, EPROM, DRAM, etc. More than 30% of premium space and 50% of the transistors could be allocated to memory alone, and the memory blocks can be located at physically diverse locations in the circuit. This mandates that to ensure reduced failure rates and increased quality, the embedded memories be tested thoroughly. However, the simultaneous increase in the complexity, density, power, and speed of these memories, compounds the testing issue and calls for special economic test methods. BIST for memories is a solution that has rapidly become popular.

SynTest's TurboBIST-Memory™, a memory BIST tool for embedded memories including SRAMs and ROMs, enables multiple BIST memory tests via a shared controller. It outputs a synthesizable RTL BIST controller and logic synthesis scripts. It also generates a Verilog testbench automatically. Diagnosis and Built-In Self-Repair features are also available.

Boundary Scan

Boundary-Scan circuitry uses only a limited number of external pins to provide physical access to various design and test modules. It can be used to access design and test modules such as IP cores, internal scan cores, and BIST cores for memory, logic or analog circuitry, within an integrated chip. Boundary-Scan can also be used to verify proper assembly on printed circuit boards or help configure a system.

SynTest's TurboBSD™, a tool for Boundary-Scan synthesis, performs IEEE 1149.1 and 1149.6 compliant Boundary-Scan logic synthesis, generates Boundary-Scan Description Language (BSDL) files and creates Boundary-Scan integrity test patterns, including verification and parametric testbenches. Verilog RTL codes are also generated for the Boundary-Scan logic.

DFT Integration and Stitching

SynTest's TurboDFT™, a tool for design integration and stitching, eliminates the tedious, error-prone manual stitching process by auto-matically integrating and stitching any combination of DFT cores, such as scan cores, memory BIST cores, logic BIST cores, analog BIST cores, IP cores, and the Boundary-Scan core. This is also general-purpose design editing and integration tool for hierarchical designs.

It automatically stitches together DFT-ready blocks created by the following SynTest DFT tools:
- Scan (VirtualScan™)
- Boundary Scan (TurboBSD™)
- Memory BIST (TurboBIST-Memory™)
- Logic BIST (TurboBIST-Logic™)

It also generates top-level testbenches for memory BIST and logic BIST cores with or without Boundary-Scan control.

Checking for Testability

SynTest's TurboCheck™, a testability checker, provides fast feed-back about potential testability and some design related problems during the design phase of the circuit, allowing changes to be made early in the design process, thereby avoiding costly iterations. To sup-port checking through the design cycle, TurboCheck comprises of TurboCheck-RTL™ for checking digital designs at RTL and TurboCheck-Gate™ for checking at the gate-level.

TurboCheck™-RTL: It identifies testability problems at the earliest stage of the design cycle, right after RTL coding. By checking the RTL codes, the designers can check for testability rule violations even before the often time-consuming logic synthesis process. The pre-logic synthesis identification of RTL design errors averts post-synthesis surprises, which result in costly and time-consuming redesign. Most testability problems can be detected at RTL coding before synthesis.

If users so desire, many DFT violations can be automatically rectified at the RTL stage in a prototype feature. This is done with minimal code insertion and minimal impact on the timing. The most common violations are generated clocks, gated set/reset, and combinational feed-back loops. This facilitates reusability of the clean RTL codes.

TurboCheck™-Gate: It is used to check the gate-level design data-base after the design is synthesized into gates. Since the RTL design has been checked by TurboCheck-RTL before synthesis, TurboCheck-Gate performs a structural-level check on the final design to further identify and zero-in on the gate-level testability violations that cannot be otherwise detected at the RTL stage.

DFT-PRO *Plus*™ in an ASIC/SoC Design Flow
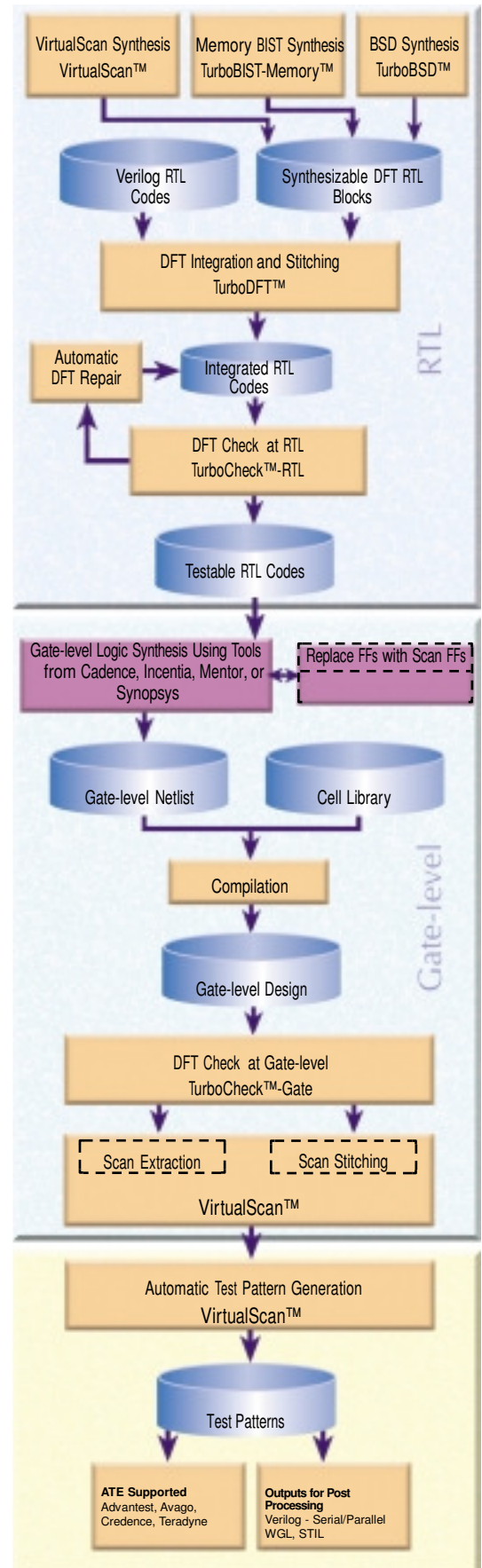
Automatic Test Pattern Generation (ATPG)

The ATPG automatically generates high quality manufacturing test patterns, producing a test program used by a specific ATE to test an IC device. The VirtualScan™ ATPG tool uses patented VirtualScan ATPG technology to generate compressed, high quality test patterns, with very high fault coverage.

The ATPG test patterns are **XteremeCompact™** (extremely compacted) for reducing test times, and are especially advantageous for multi-frequency, multi-clock designs. The ATPG test patterns are available in various formats for post processing.

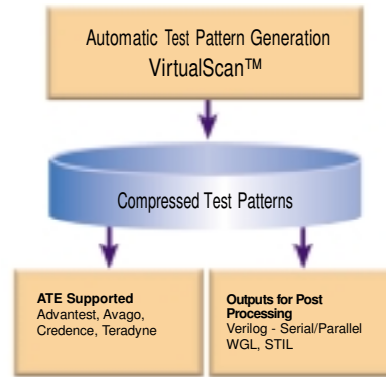## Scan Test for a Multiple-Capture-per-Cycle Scheme

SynTest's patented multiple-capture-per-cycle scheme for ATPG slashes the total test time of multi-frequency, multi-clock domain designs, as all clock domains are captured in each capture cycle.

Fault Coverage

VirtualScan™ allows the user to configure its architecture to meet fault coverage requirements. To ensure no loss in fault coverage, the user can initially run the ATPG using VirtualScan mode and subsequently run it as serial scan mode. Even in this case, significant reductions are available in the test data volume and the test cycle volume.

PLATFORMS DFT-PRO *Plus*™ package runs on Linux.

PATENTS SynTest products are protected by one or more of the patents listed in http://syntest.com/patent.htm. Patents pending in the U.S. and other countries.

ORDERING INFORMATION

DFT-PRO *PLUS*™ (INCLUDES)
- TurboBSD™: For Boundary-Scan Synthesis
- TurboBIST-Memory™: For Memory BIST Synthesis
- TurboDFT™: For design/DFT Integration
- TurboCheck™: For DFT Rule Checking and Repair
- VirtualScan™: For VirtualScan Synthesis and VirtualScan ATPG
- ATE Test Program Outputs

Other Products from SynTest
- TurboBIST-Logic™: Logic BIST Tool Suite
- TurboFault™: Concurrent Fault Simulator
- TurboDiagnosis™: ATE-based Fault Diagnosis on SoCs
- TurboDeskTopDebugger™: PC-Based Fault Diagnosis on SoCs

Automatic Test Pattern Generation
VirtualScan™

Compressed Test Patterns

ATE Supported
Advantest, Avago, Credence, Teradyne

Outputs for Post Processing
Verilog - Serial/Parallel
WGL, STIL

OTHER PRODUCTS from SYNTEST

TurboBIST-Logic™
- Helps reduce ATE tester costs during production, by using at-speed testing. Ideal when dealing with SoC designs with multi-million gates, multiple clock domains, and multiple frequencies including high frequencies.
- Helps improve quality of deep sub-micron chips by detecting at-speed, delay faults.
- Offers comprehensive fault detection when testing circuits with multiple clocks and multiple frequencies using SynTest's patented capture scheme for true multi-frequency, multi-clock handling.
- Helps reduce design time and test costs as well as ensures higher quality and reliability when using multiple instantiations of "legacy" logic circuit blocks or re-using IP cores in different designs.
- Helps in the wafer sorting process and thereby helps in reducing packaging costs.
- Ideal for in-field remote testing or non-invasive testing of crucial electronic products.
- Helps during prototype debug / diagnosis.

TurboFault™

It is the fastest, high capacity concurrent fault simulator based on the latest advances in cycle-based simulation technology. With its low memory consumption, user-definable fault detection criteria, fault-tracing, back-tracing, and crash recovery capabilities, it combines high performance with versatility and accuracy.

It accepts fault lists from most ATPG tools. As input stimuli, it can handle VCD, WGL and Springsoft FSDB. It can take full timing designs with SDF and supports synchronous and asynchronous designs at gate level. Consult SynTest for behavioral-level concurrent fault simulation.

SYNTEST

Corporate Headquarters:

SynTest Technologies, Inc.
505 S. Pastoria Ave., Suite 101
Sunnyvale, CA 94086, USA

Telephone: +1.408.720.9956
Facsimile: +1.408.720.9960
E-Mail: info@syntest.com

Offices and Distributors Worldwide -- Please call, e-mail or visit our web site for the one closest to you.
http://www.syntest.com